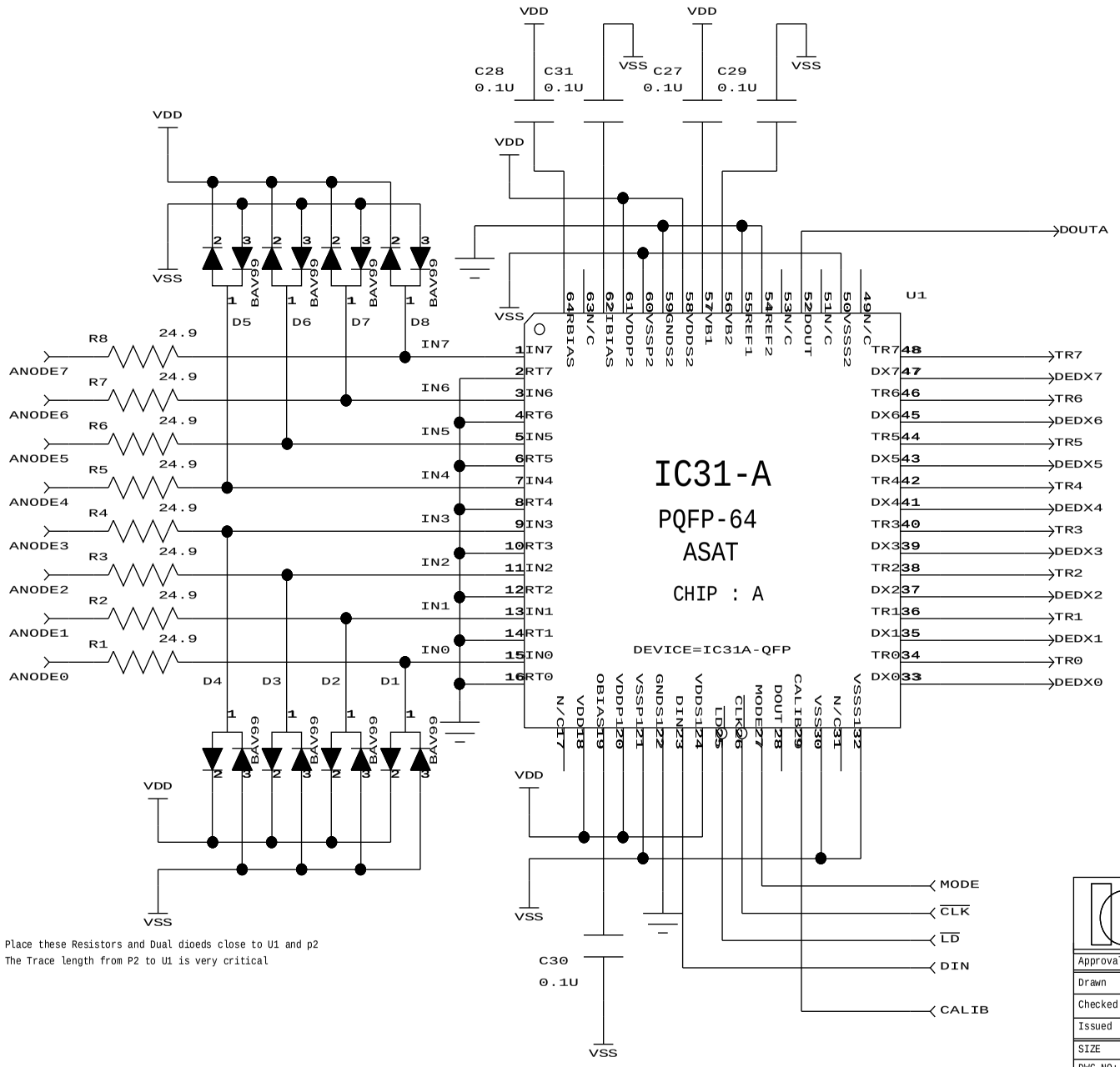

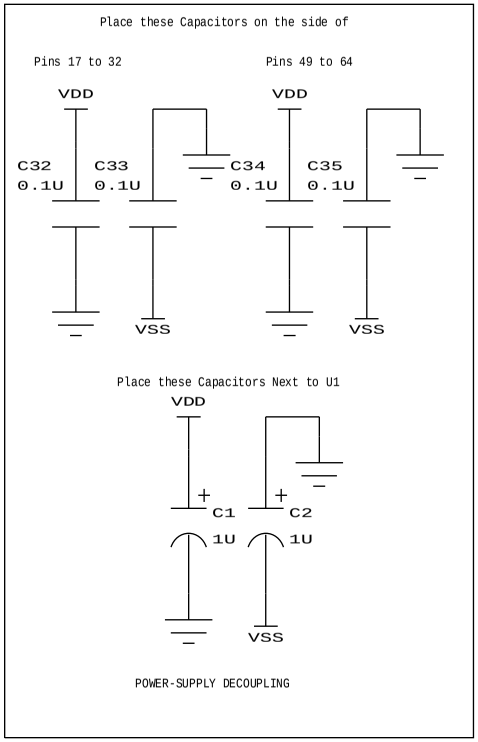

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Approvals / Date	Drawing: PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Drawn	
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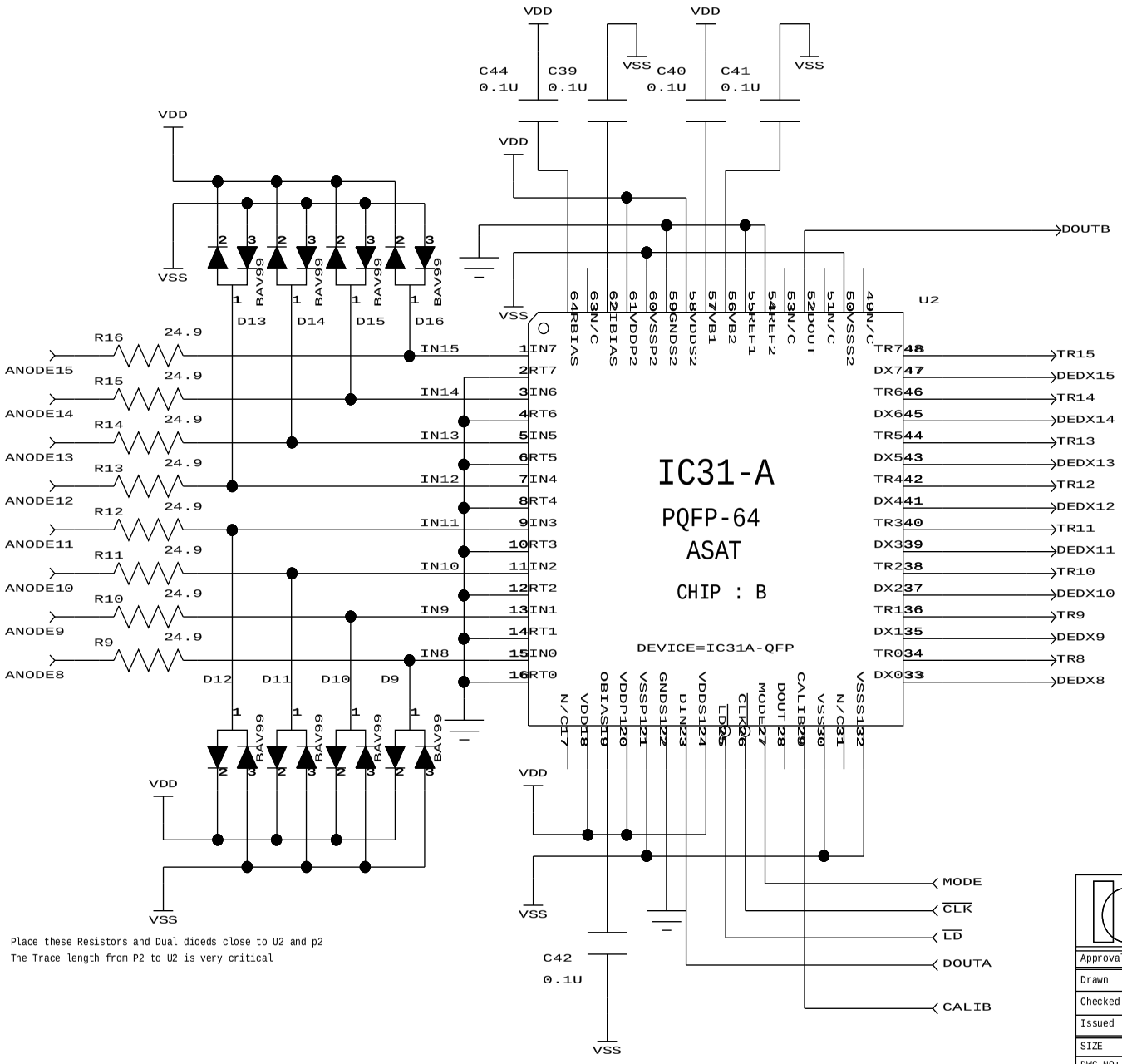
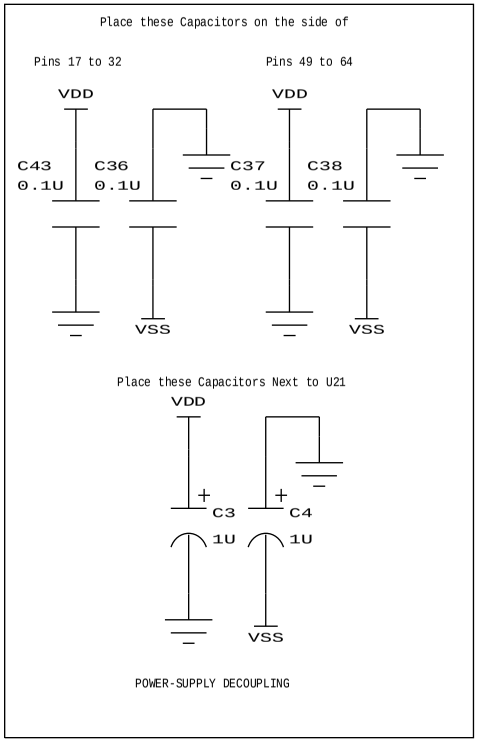
SIZE: B	TECPS Rev2 - 32 Channels
DWG NO:	
REV NO: 1	
SCALE	
Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov	
Sheet: 1 of 46	





Place these Resistors and Dual dioeds close to U2 and p2
The Trace length from P2 to U2 is very critical

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@DATETIME=8-25-1997_15:29

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels

Drawn By:
Anand Kandasamy
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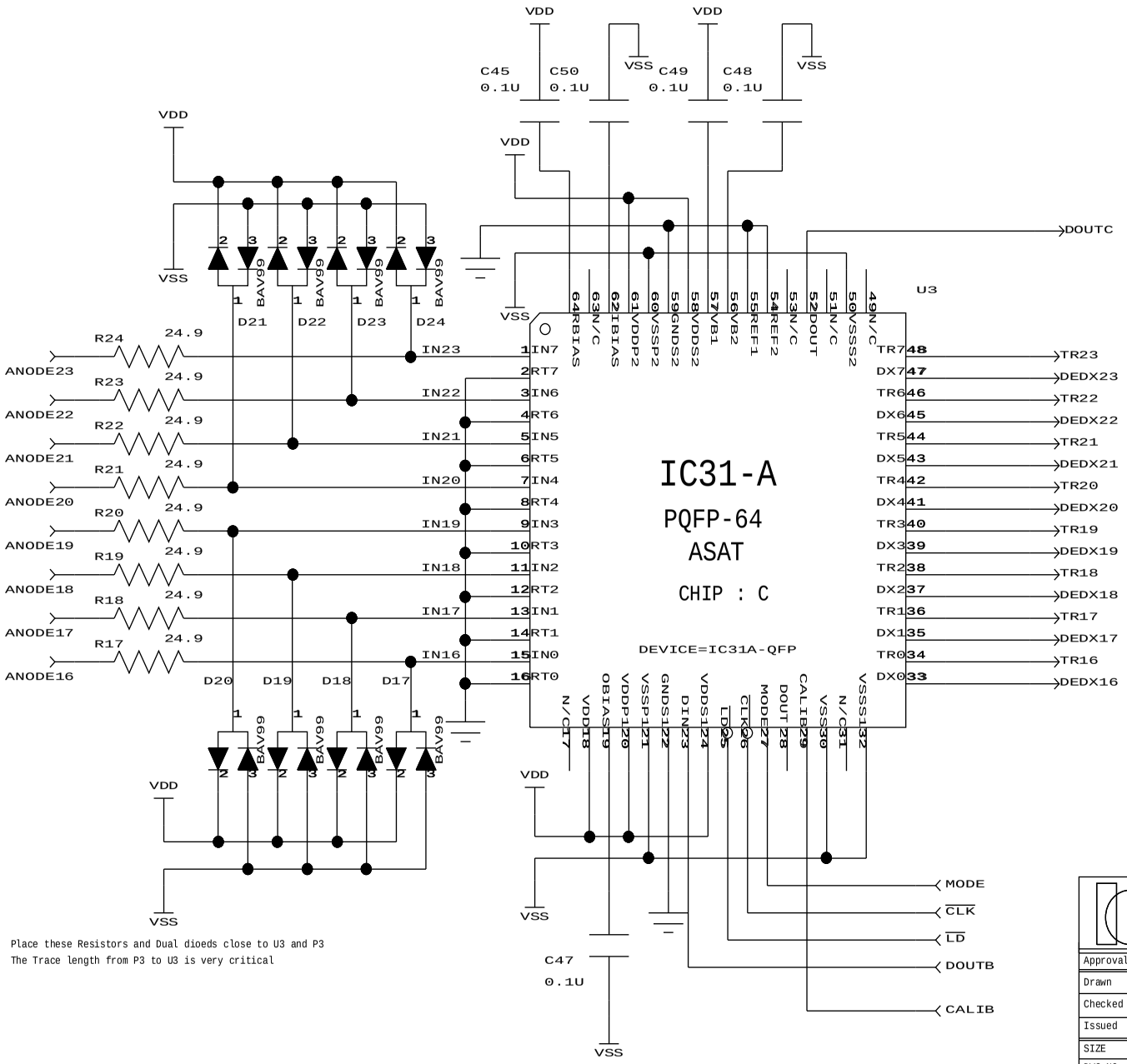

Place these Resistors and Dual dioeds close to U3 and P3
The Trace length from P3 to U3 is very critical

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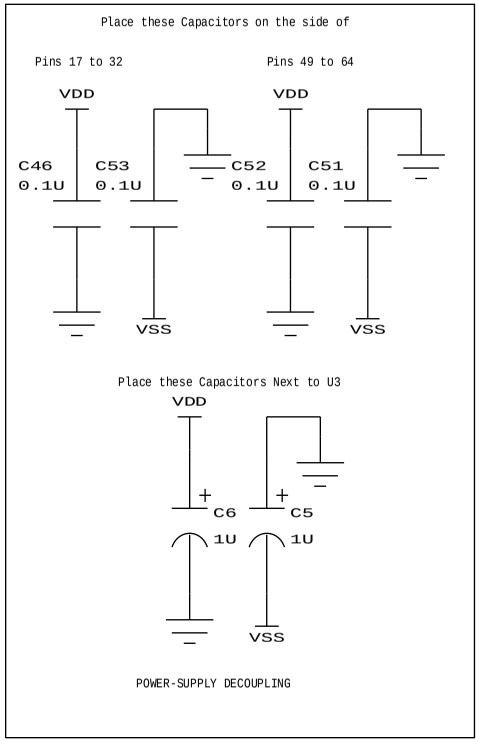

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels

Drawn By:
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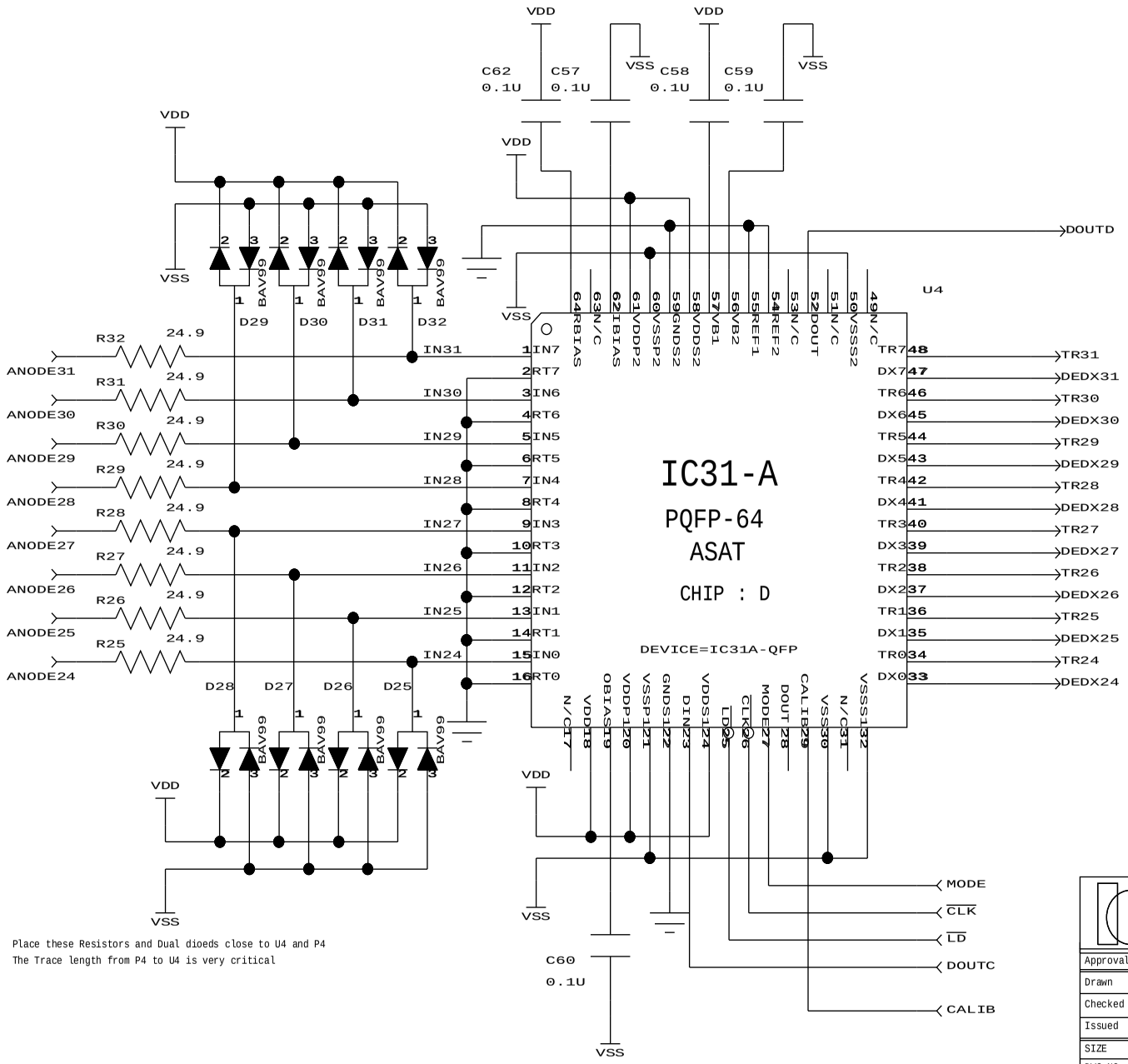

Place these Resistors and Dual dioeds close to U4 and P4
The Trace length from P4 to U4 is very critical

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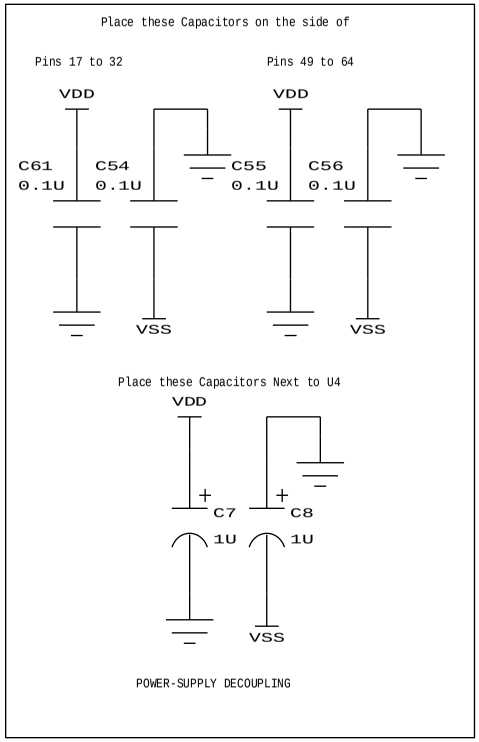

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels

Drawn By:
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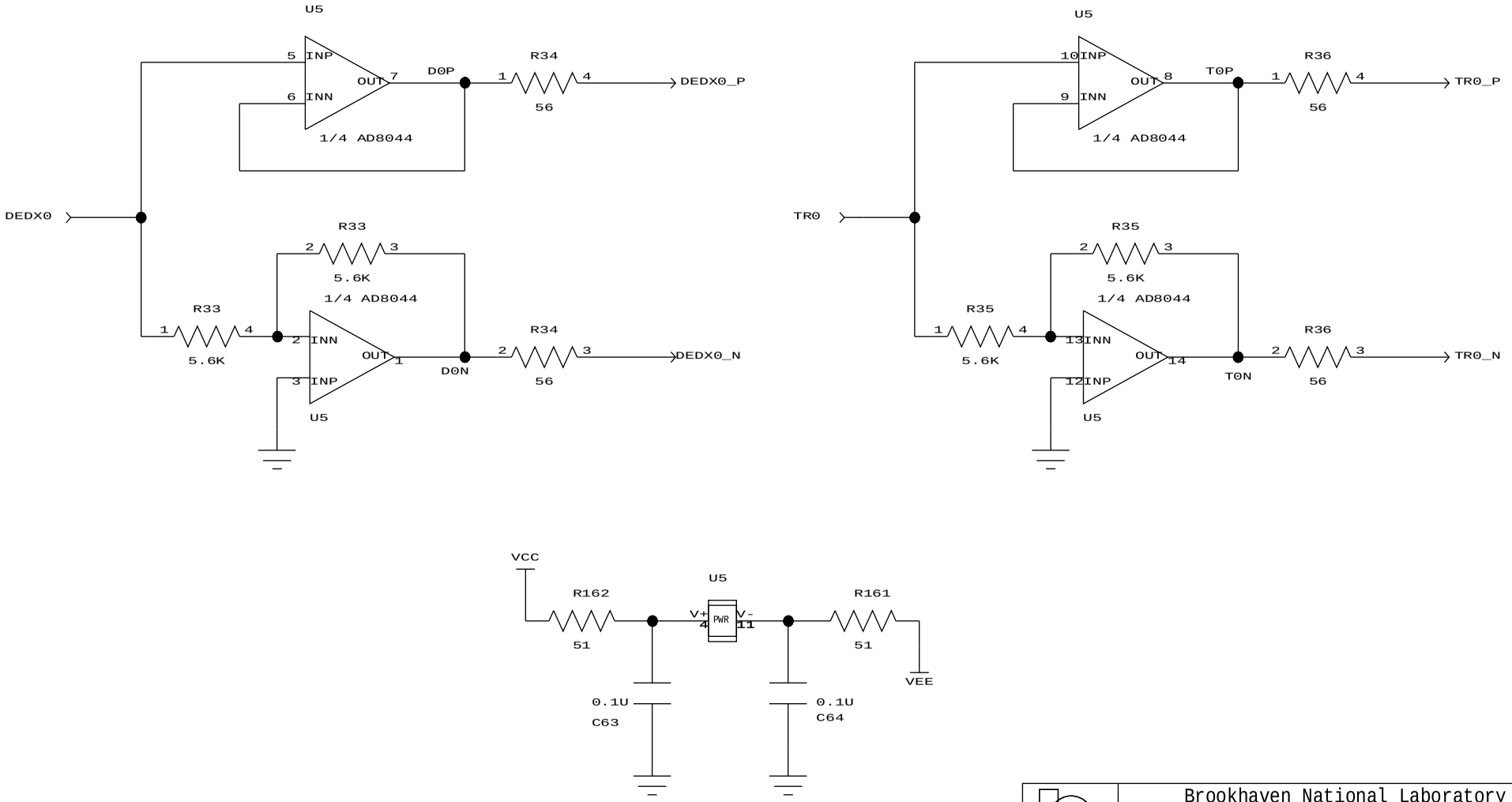

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 0; TR and dE/dX

Drawn By:
Anand Kandasamy
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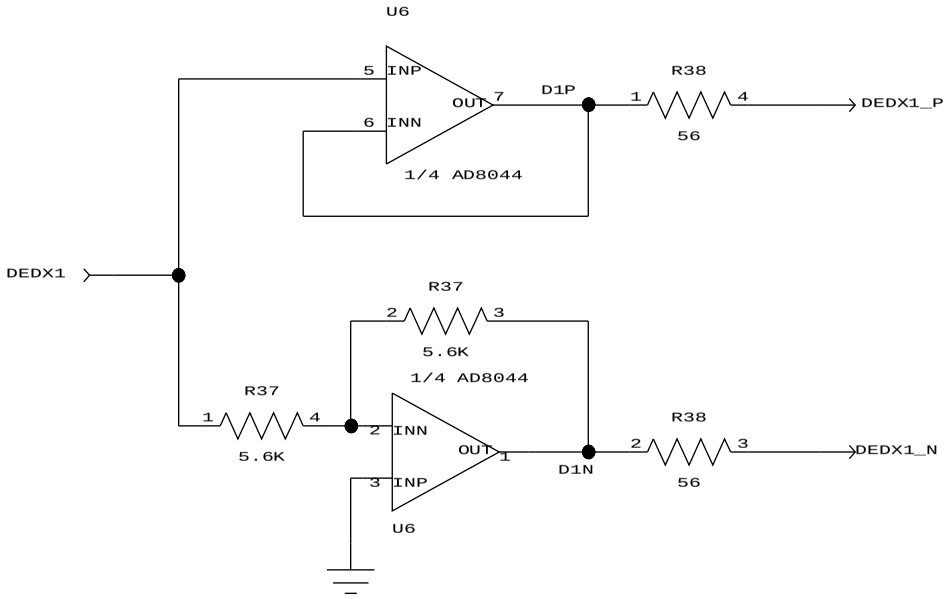

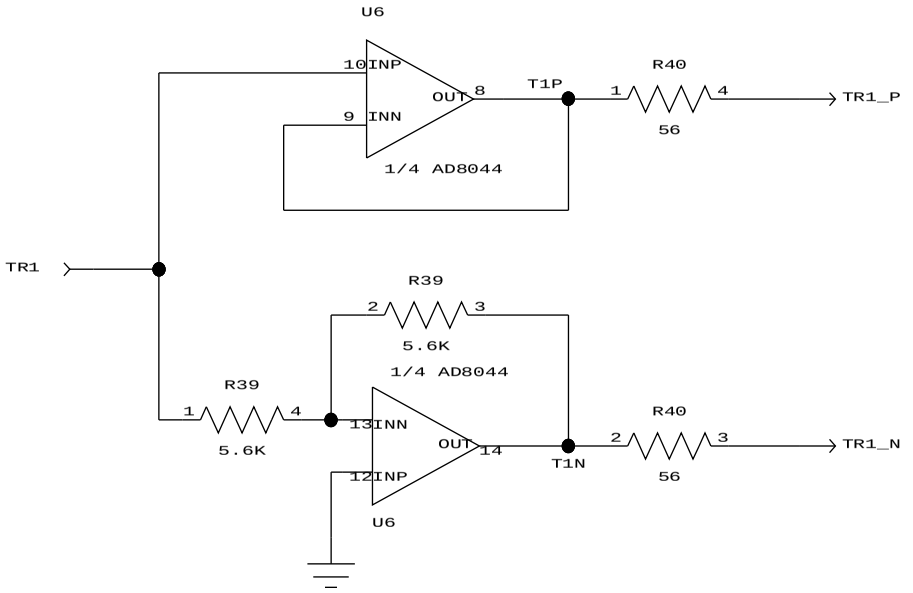

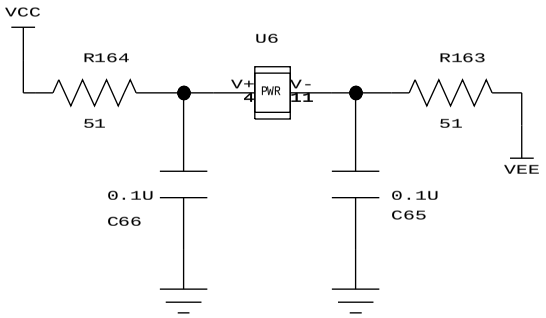

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SIZE: B DWG NO: REV NO: 1 SCALE	TECPS Rev2 - 32 Channels Channel 1; TR and dE/dX
Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov	Sheet: 6 of 46

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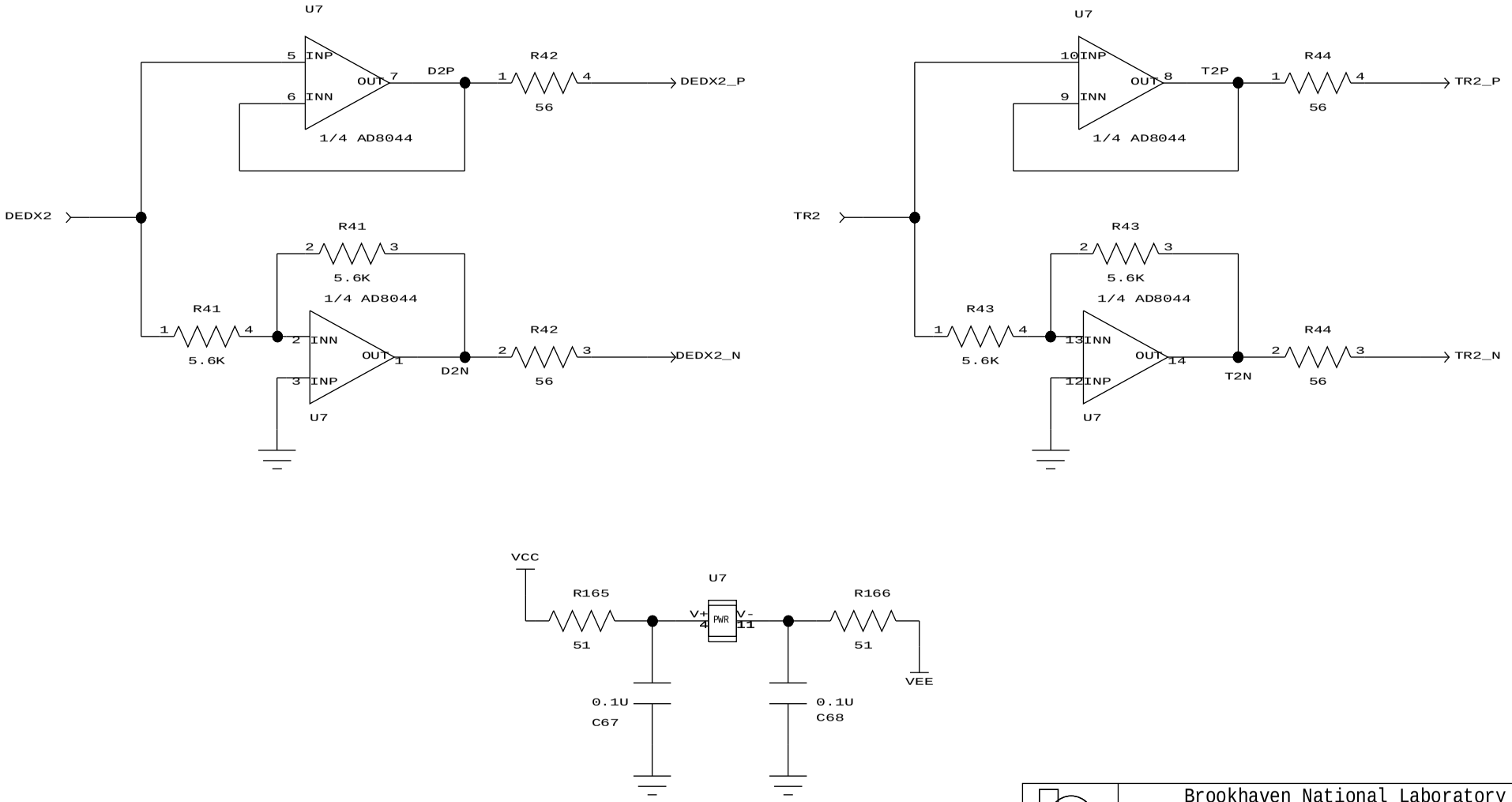

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 2; TR and dE/dX

Drawn By:
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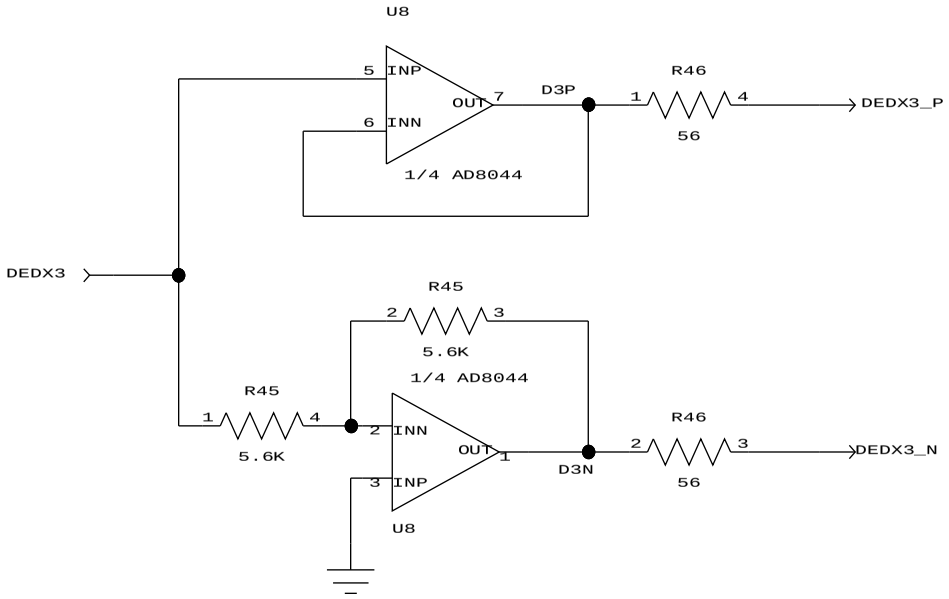

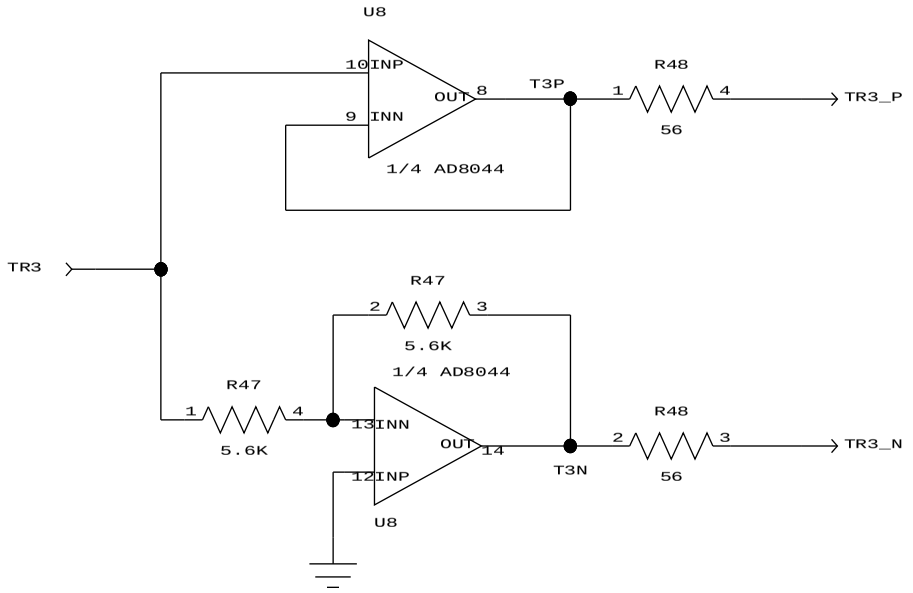

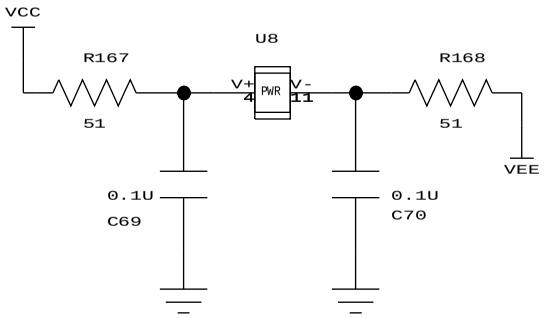

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 3; TR and dE/dX

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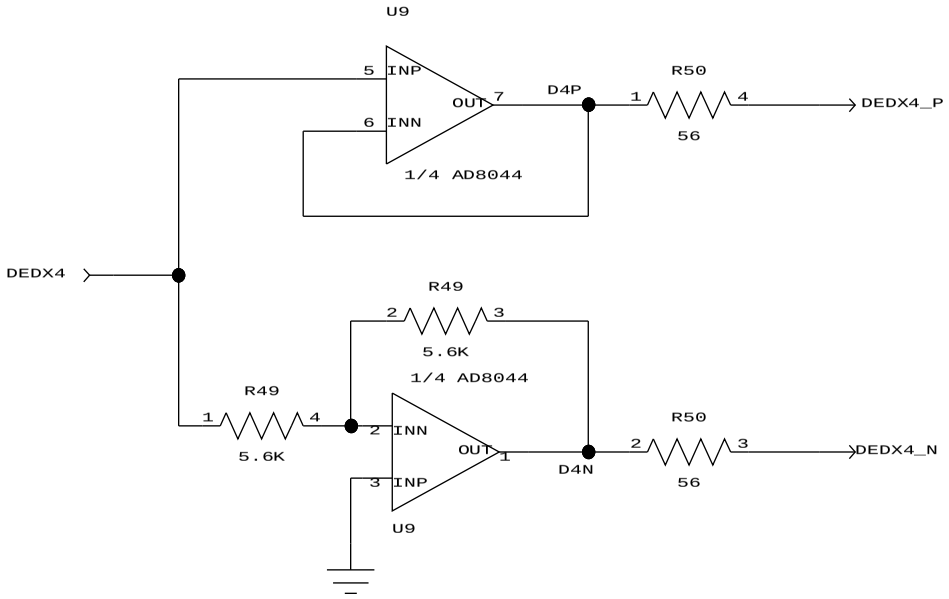

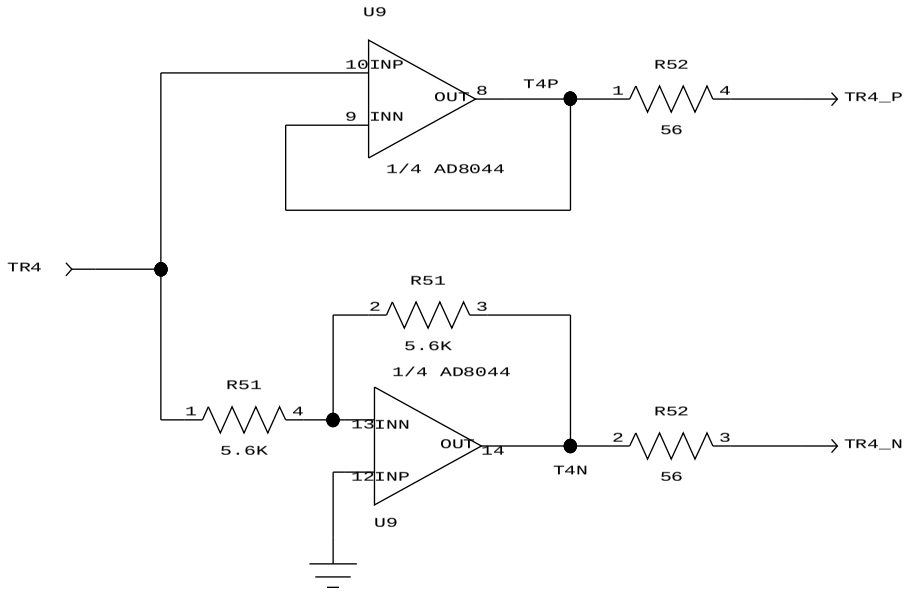

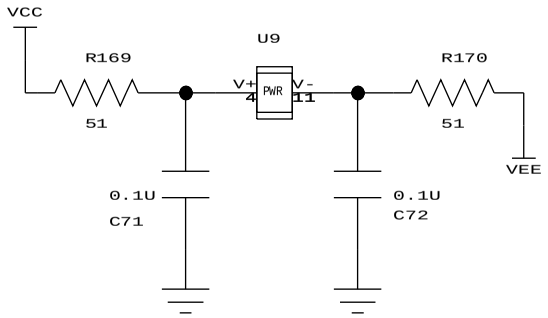

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 4; TR and dE/dX

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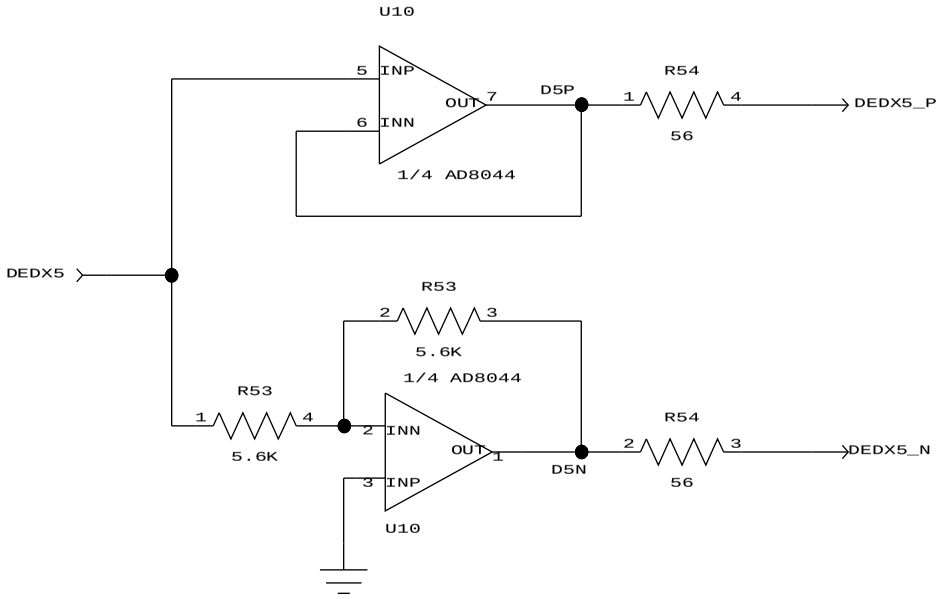

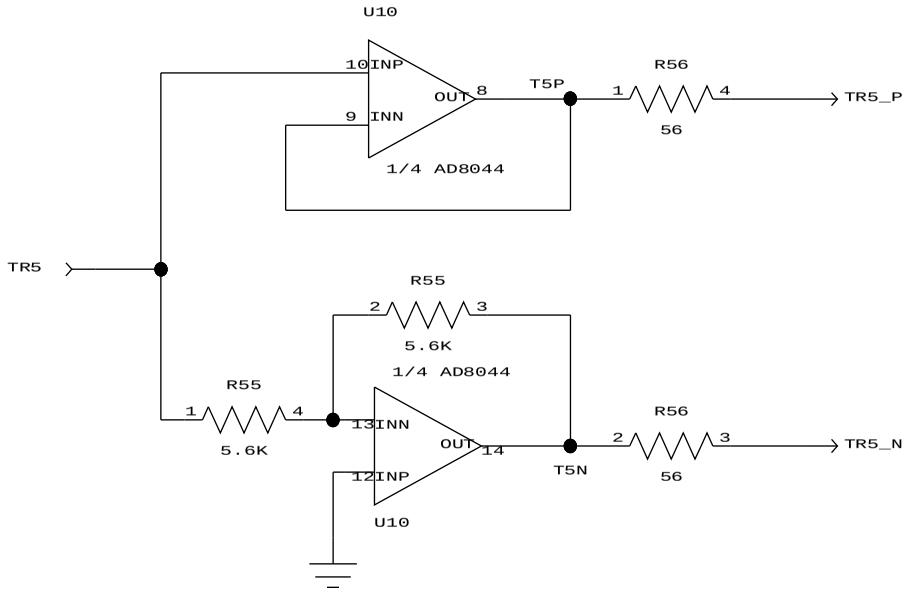

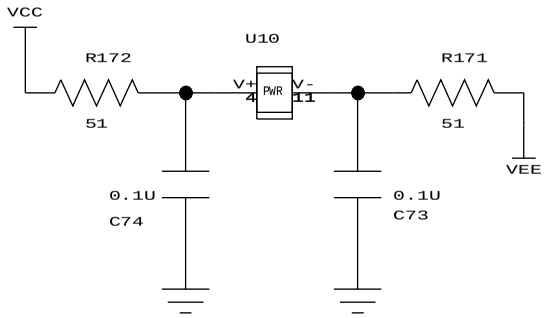

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 5; TR and dE/dX

Drawn By:
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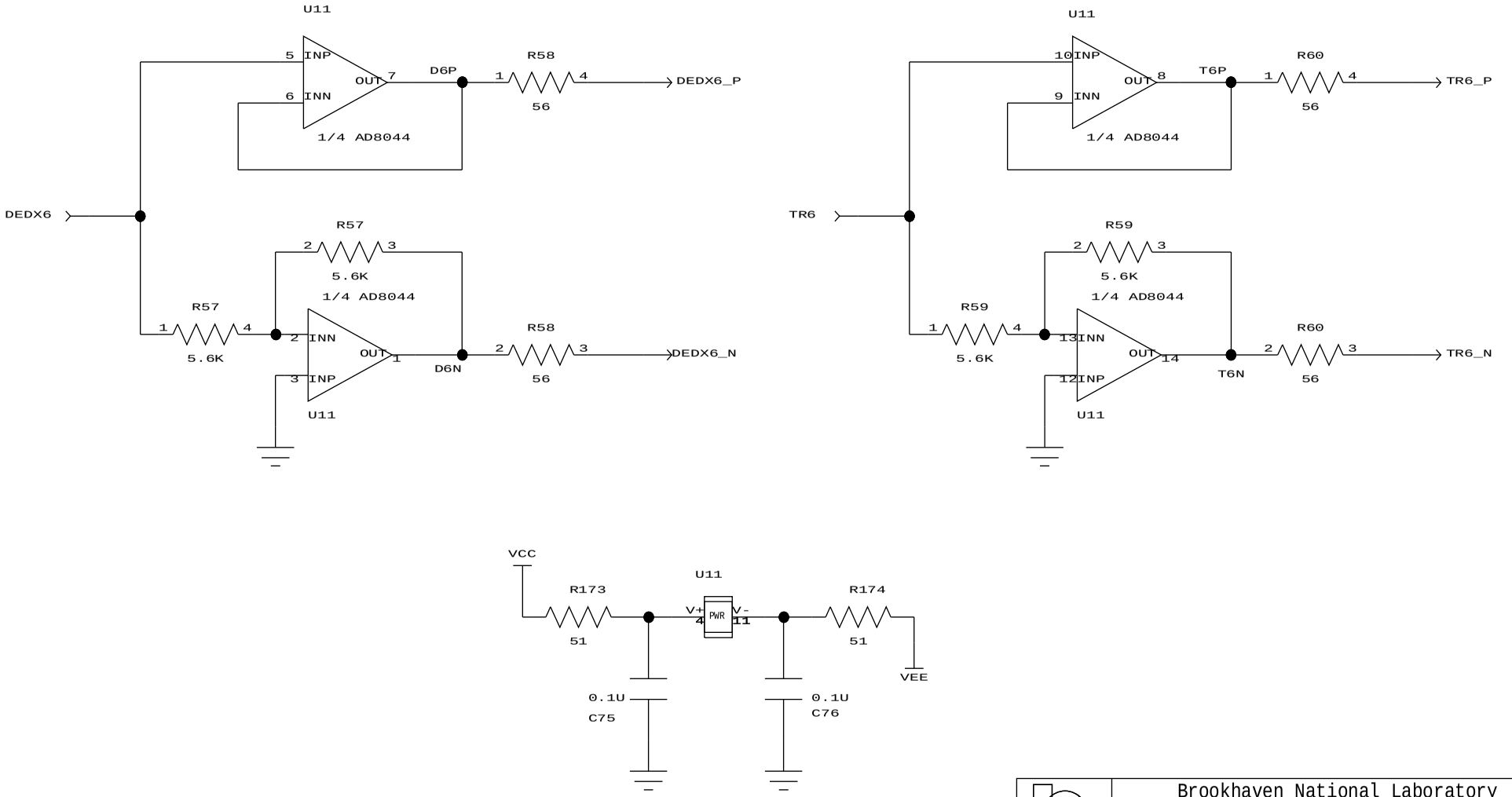

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 6; TR and dE/dX

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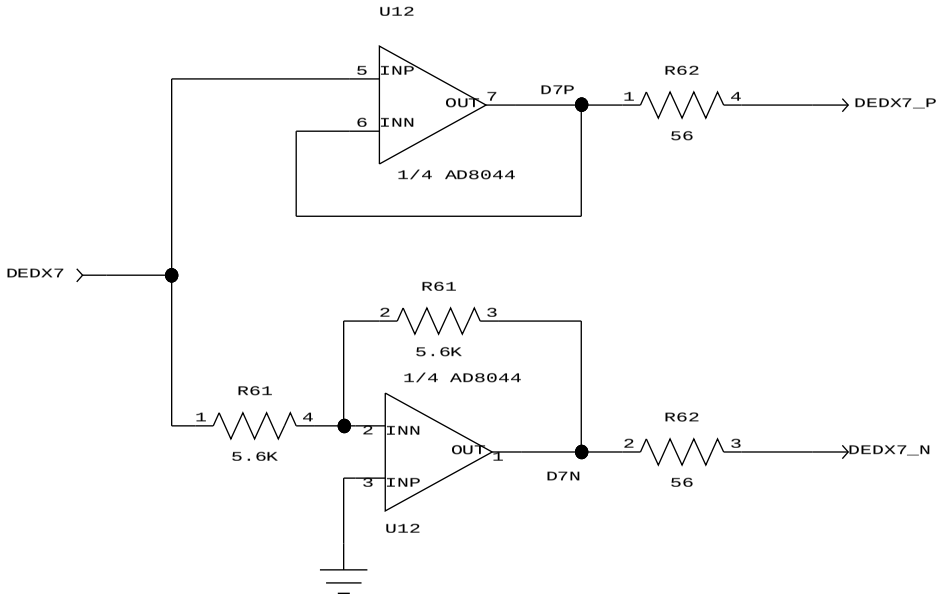

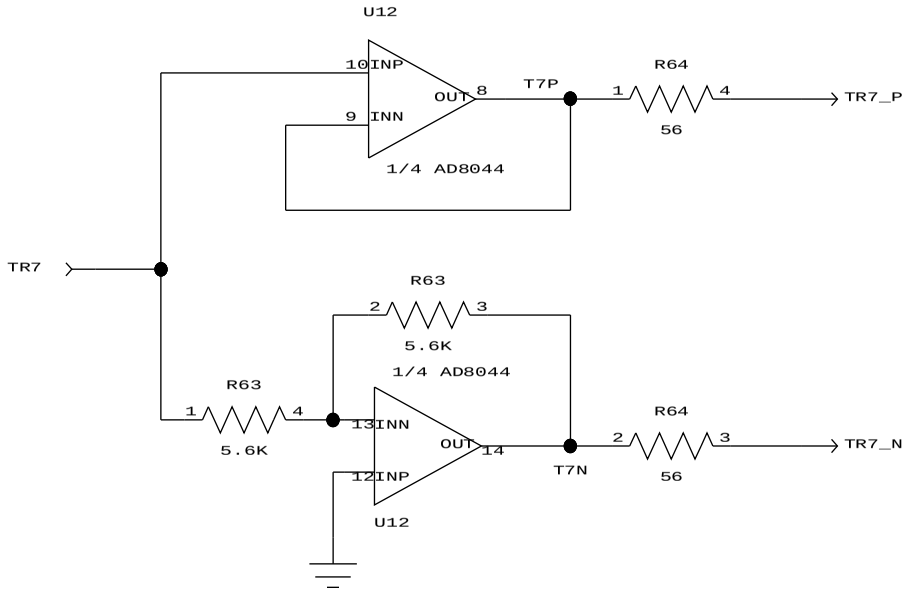

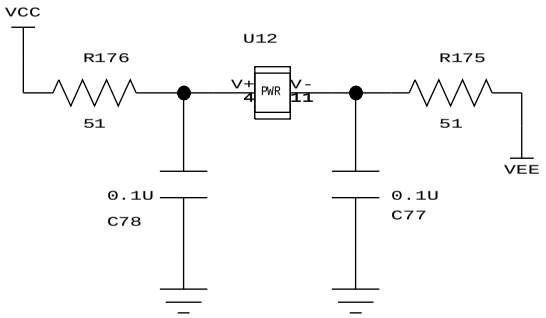

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 7; TR and dE/dX

Drawn By:
Anand Kandasamy
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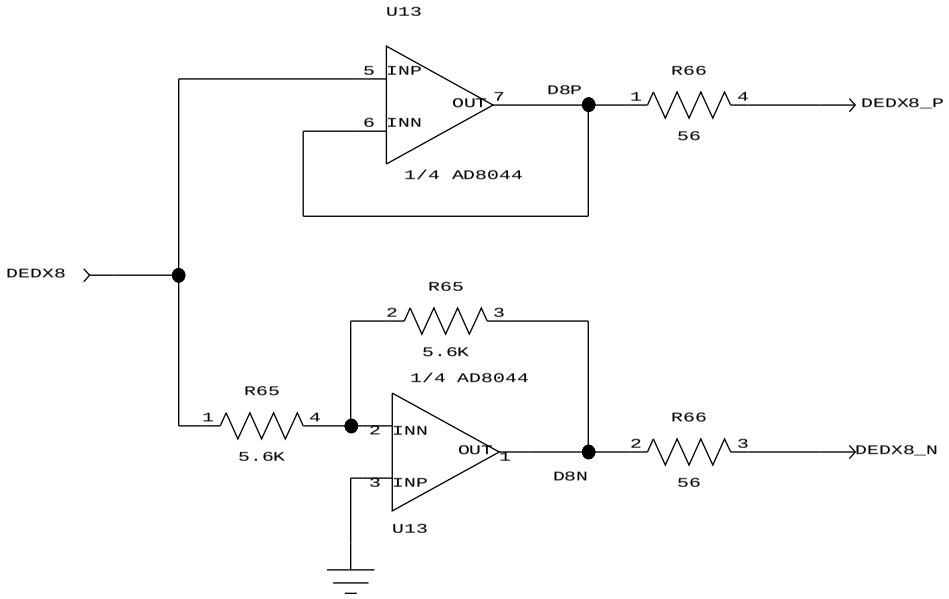

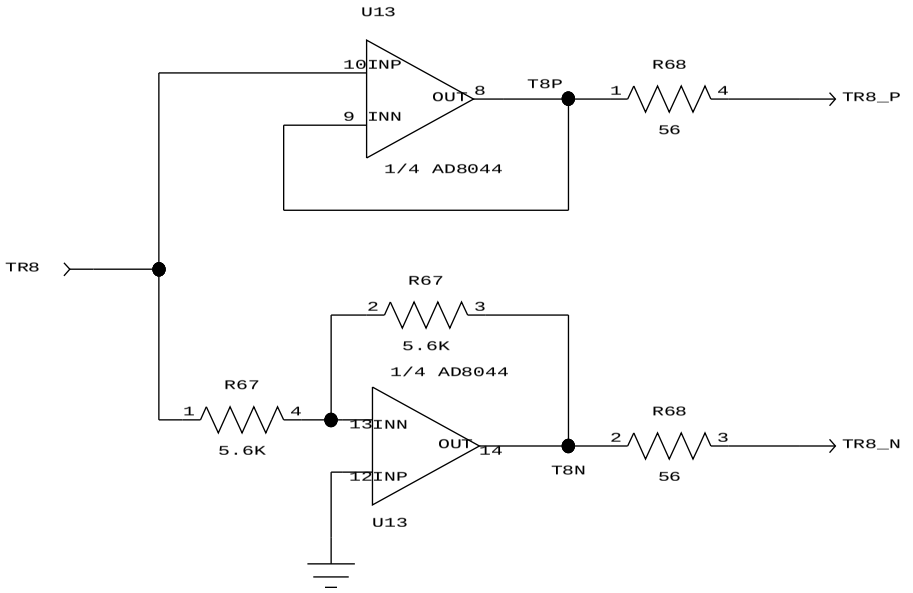

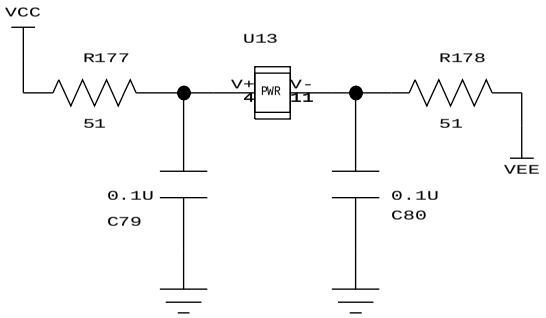

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Approvals / Date	Drawing: PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Drawn	
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SIZE: B DWG NO: REV NO: 1 SCALE	TECPS Rev2 - 32 Channels Channel 8; TR and dE/dX
Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov	Sheet: 13 of 46

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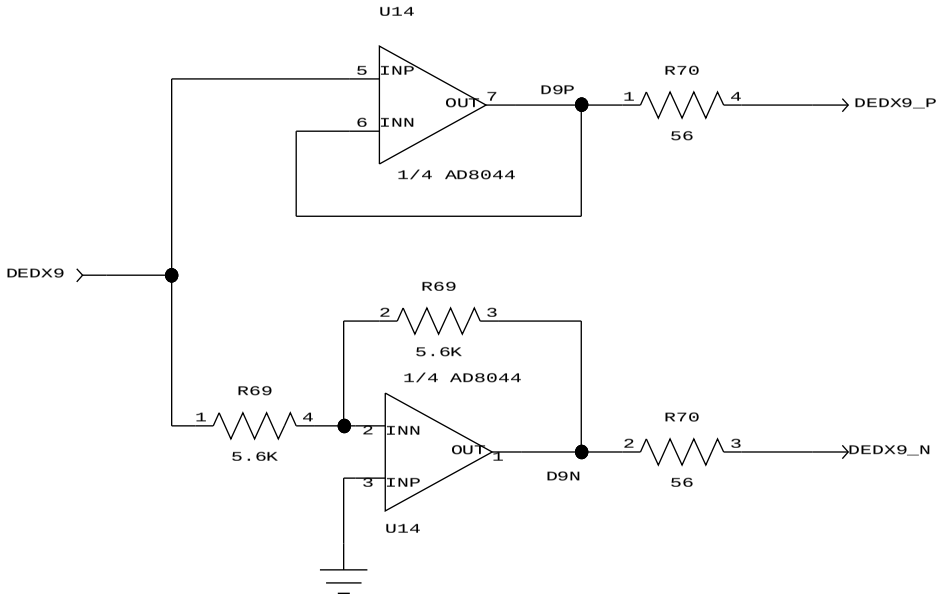

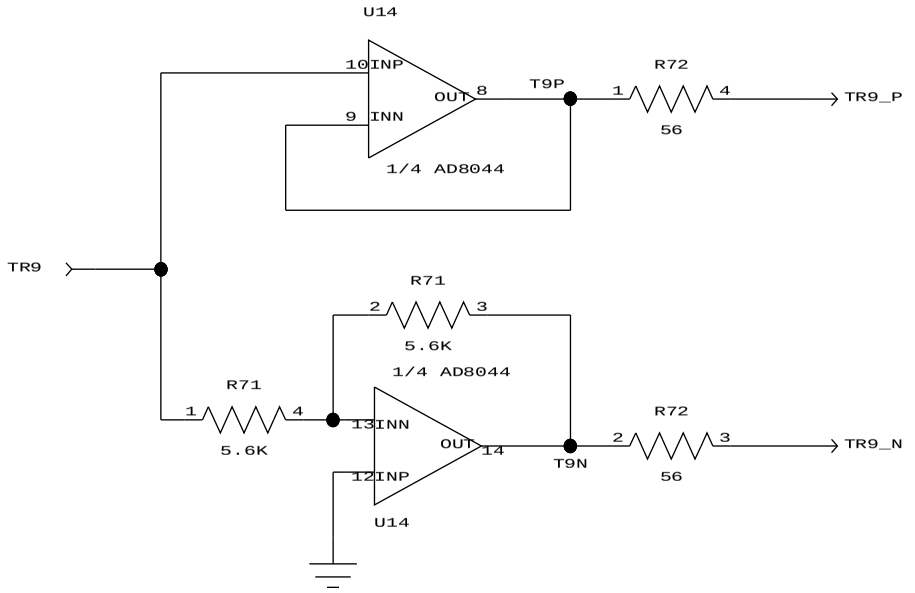

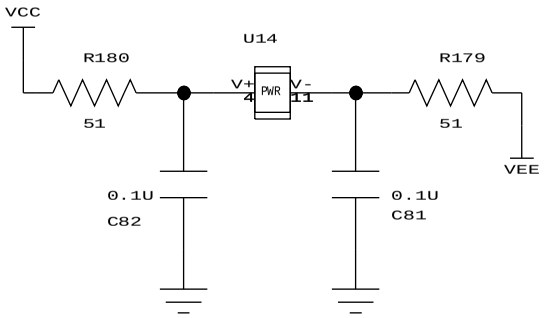

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 9; TR and dE/dX

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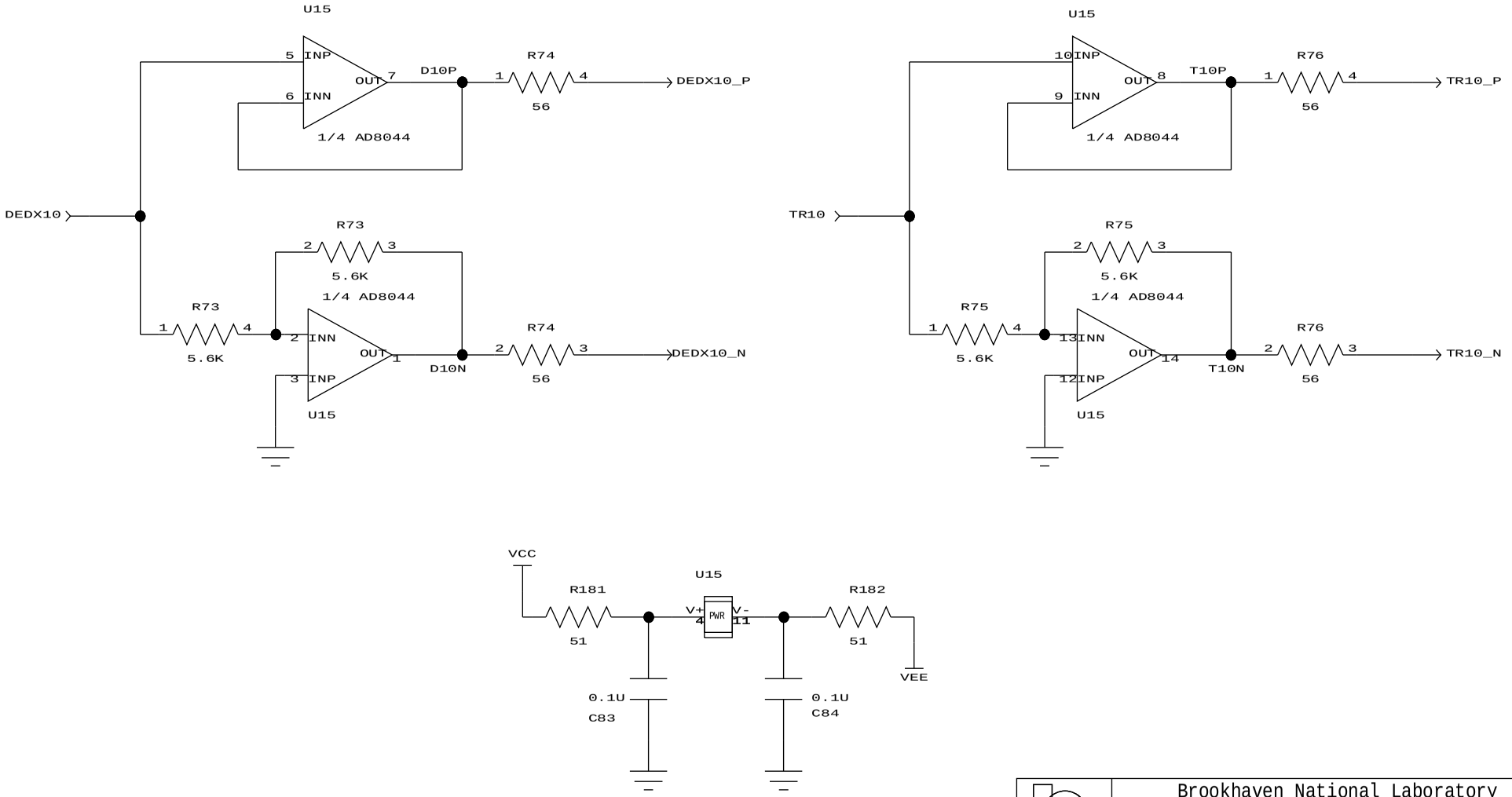

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 10; TR and dE/dX

Drawn By:
Anand Kandasamy
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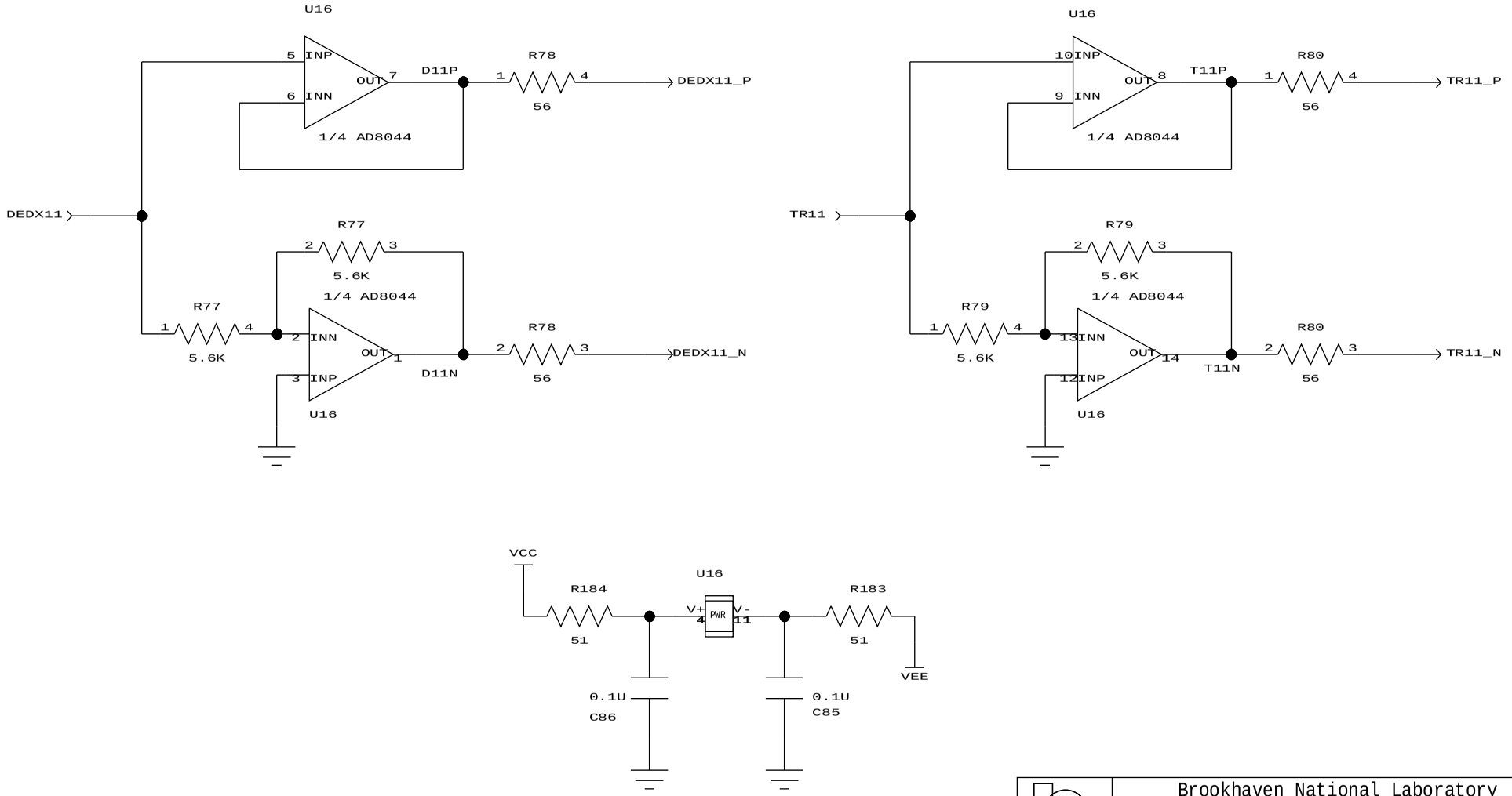

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 11; TR and dE/dX

Drawn By:
Anand Kandasamy
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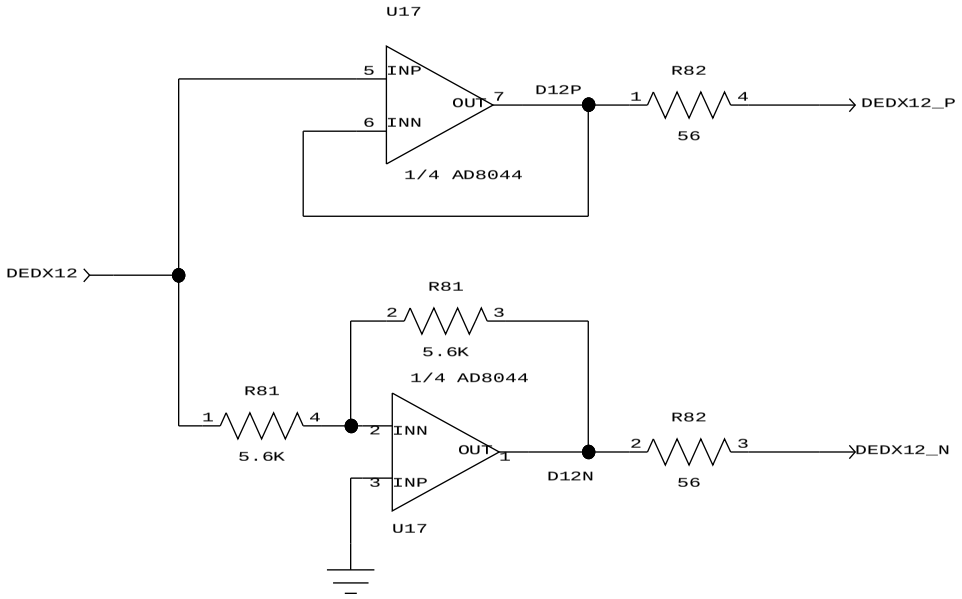

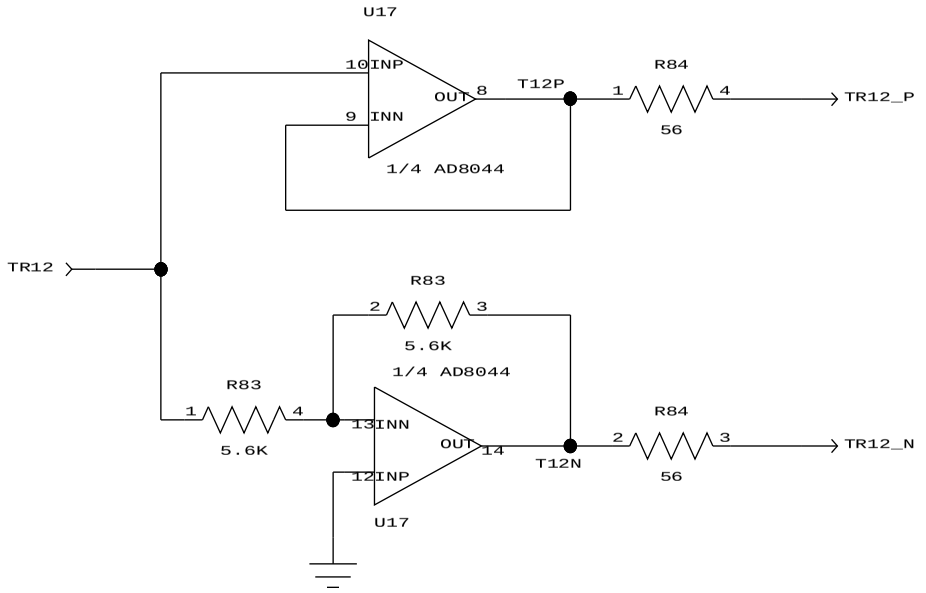

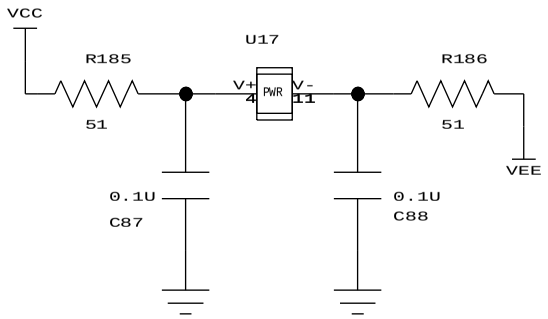

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PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 12; TR and dE/dX

Drawn By:
Anand Kandasamy
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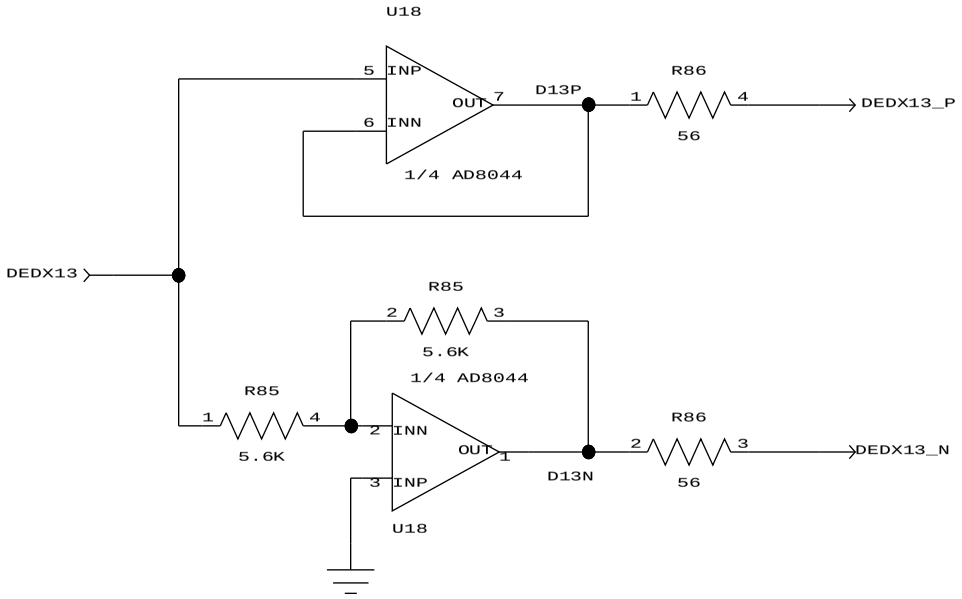

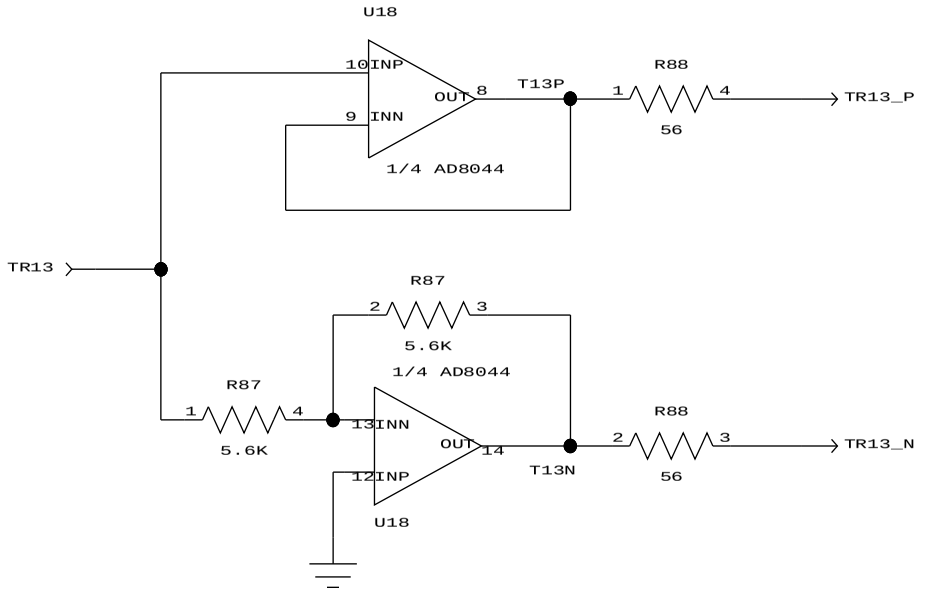

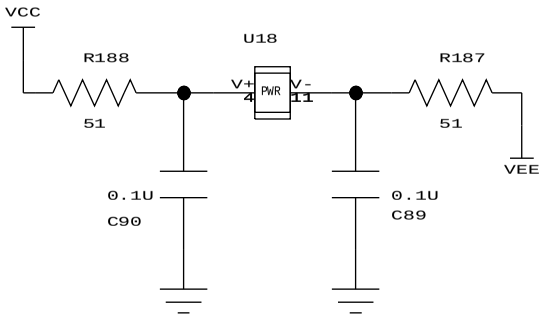

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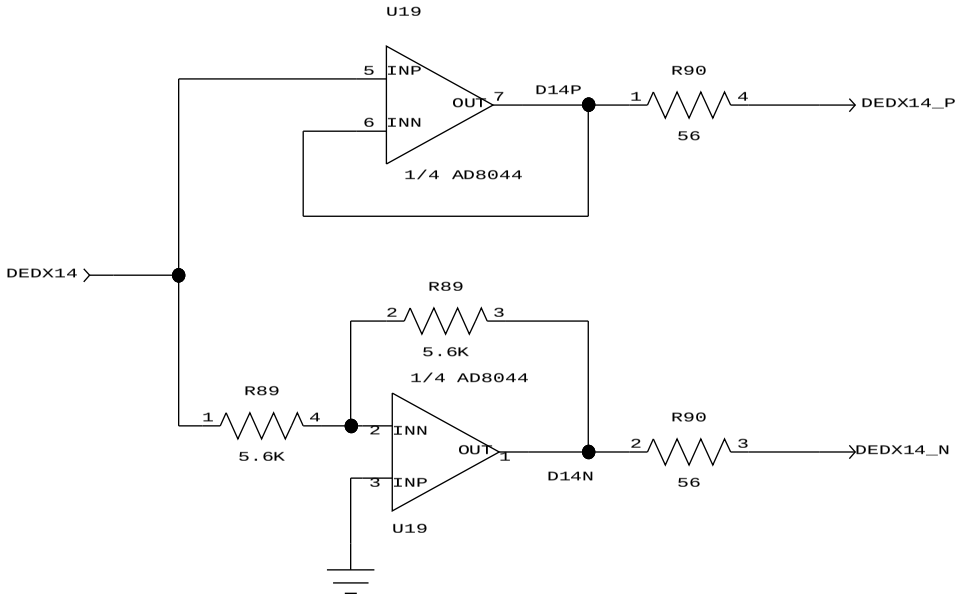
Approvals	Date
Drawn	
Checked	
Issued	

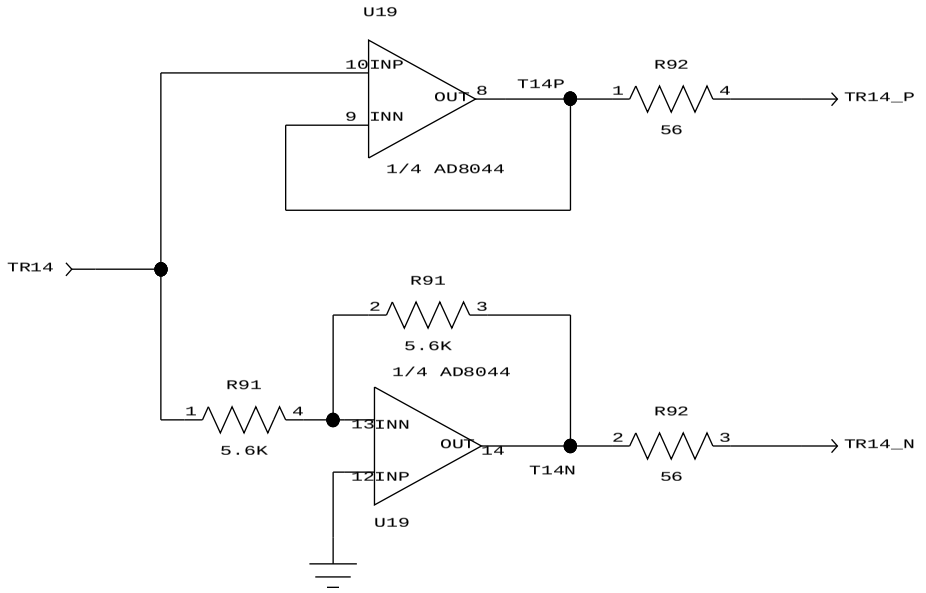
Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

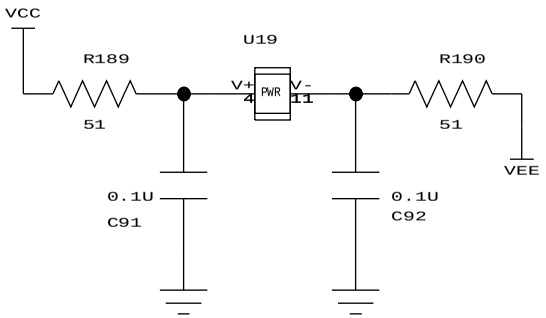
SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 13; TR and dE/dX

Drawn By:
Anand Kandasamy
516-344-5486
anand@bnl.gov







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@DATETIME=10-27-1997_13:00

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Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 14; TR and dE/dX

Drawn By:
Anand Kandasamy
516-344-5486
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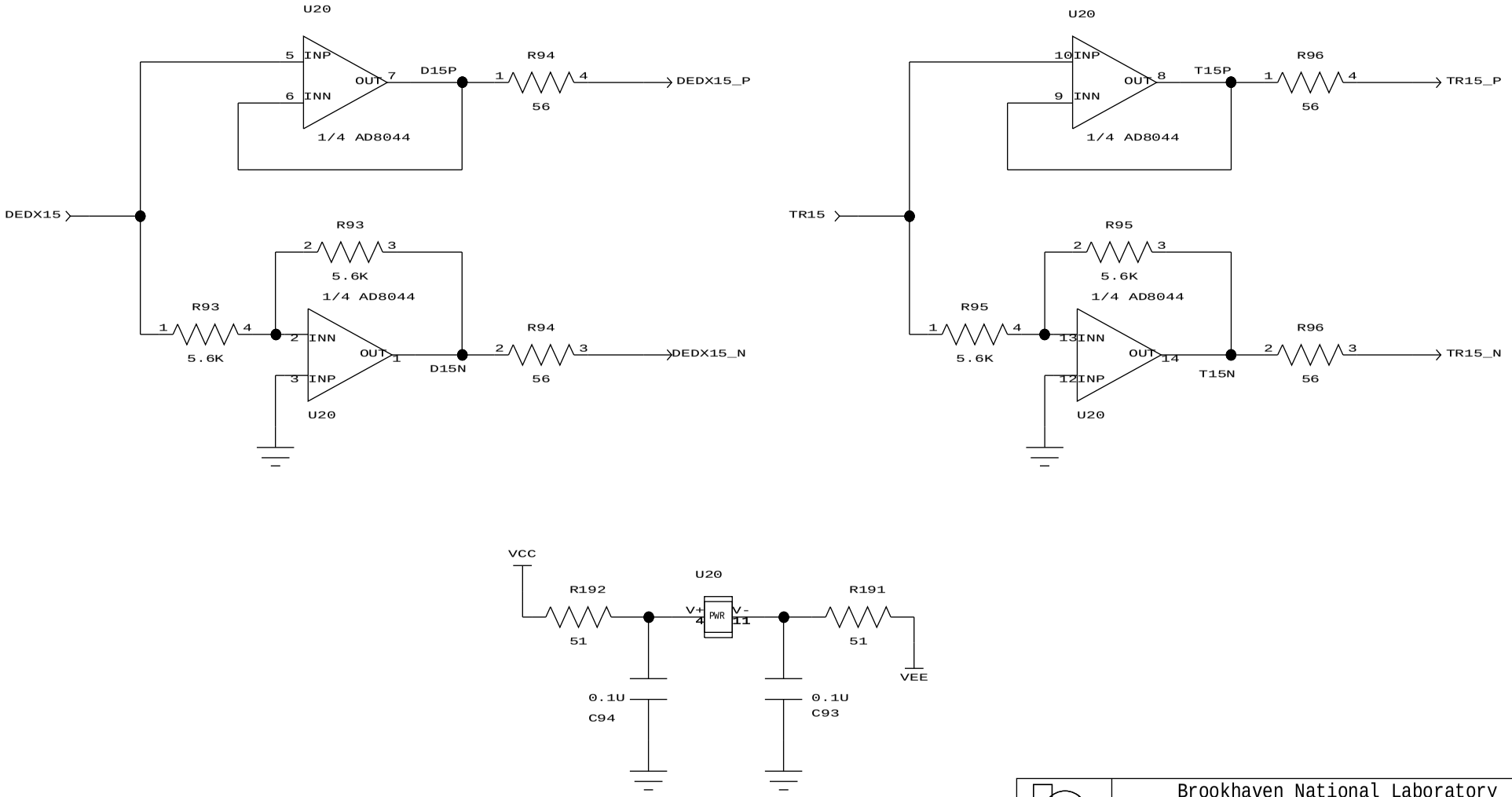

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@DATETIME=10-27-1997_13:00

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Instrumentation Division
Upton, NY 11973

Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 15; TR and dE/dX

Drawn By:
Anand Kandasamy
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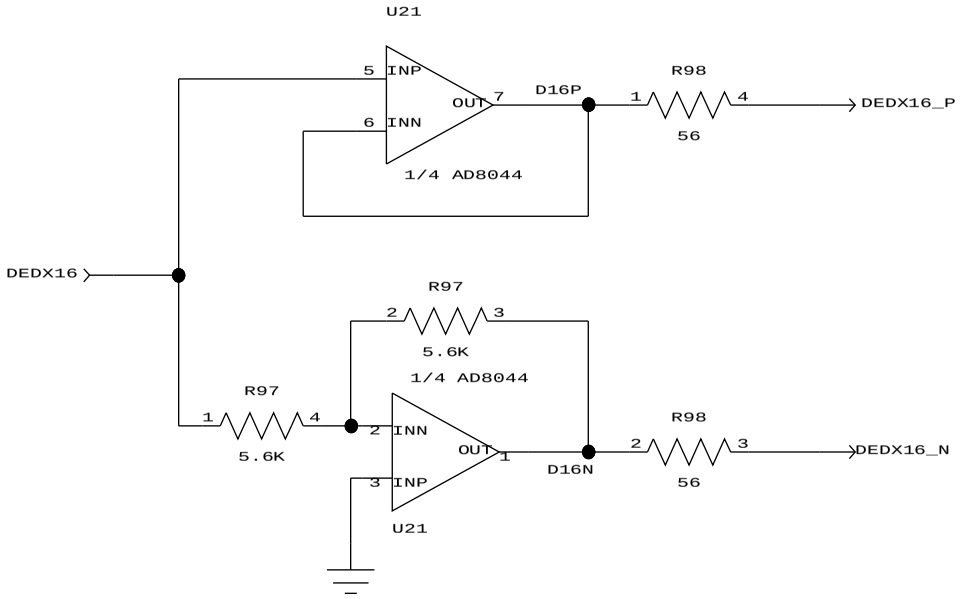

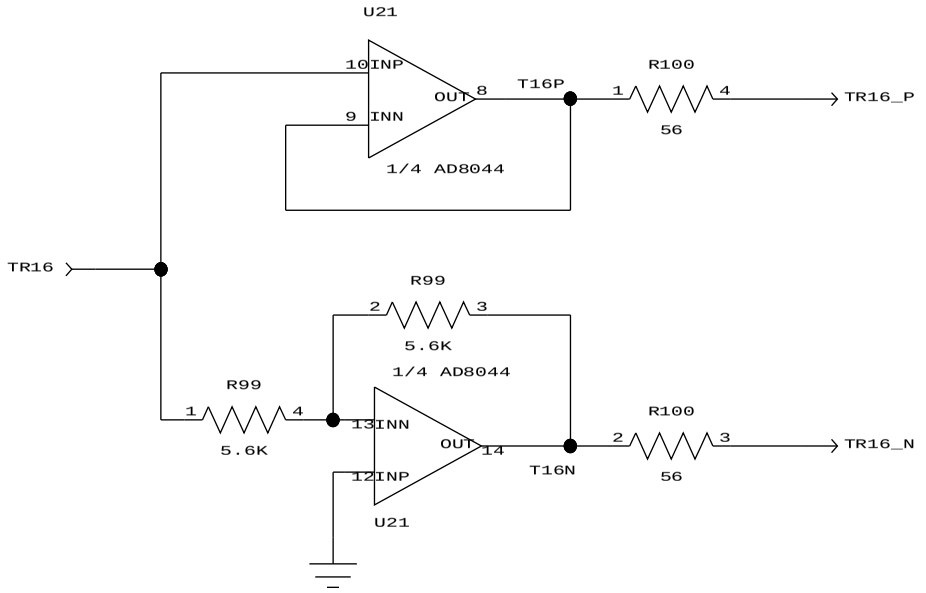

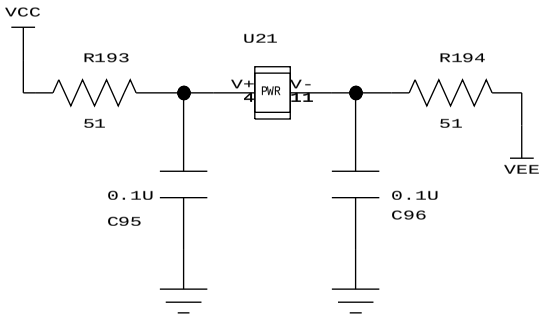

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@DATETIME=10-27-1997_13:00

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Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 16; TR and dE/dX

Drawn By:
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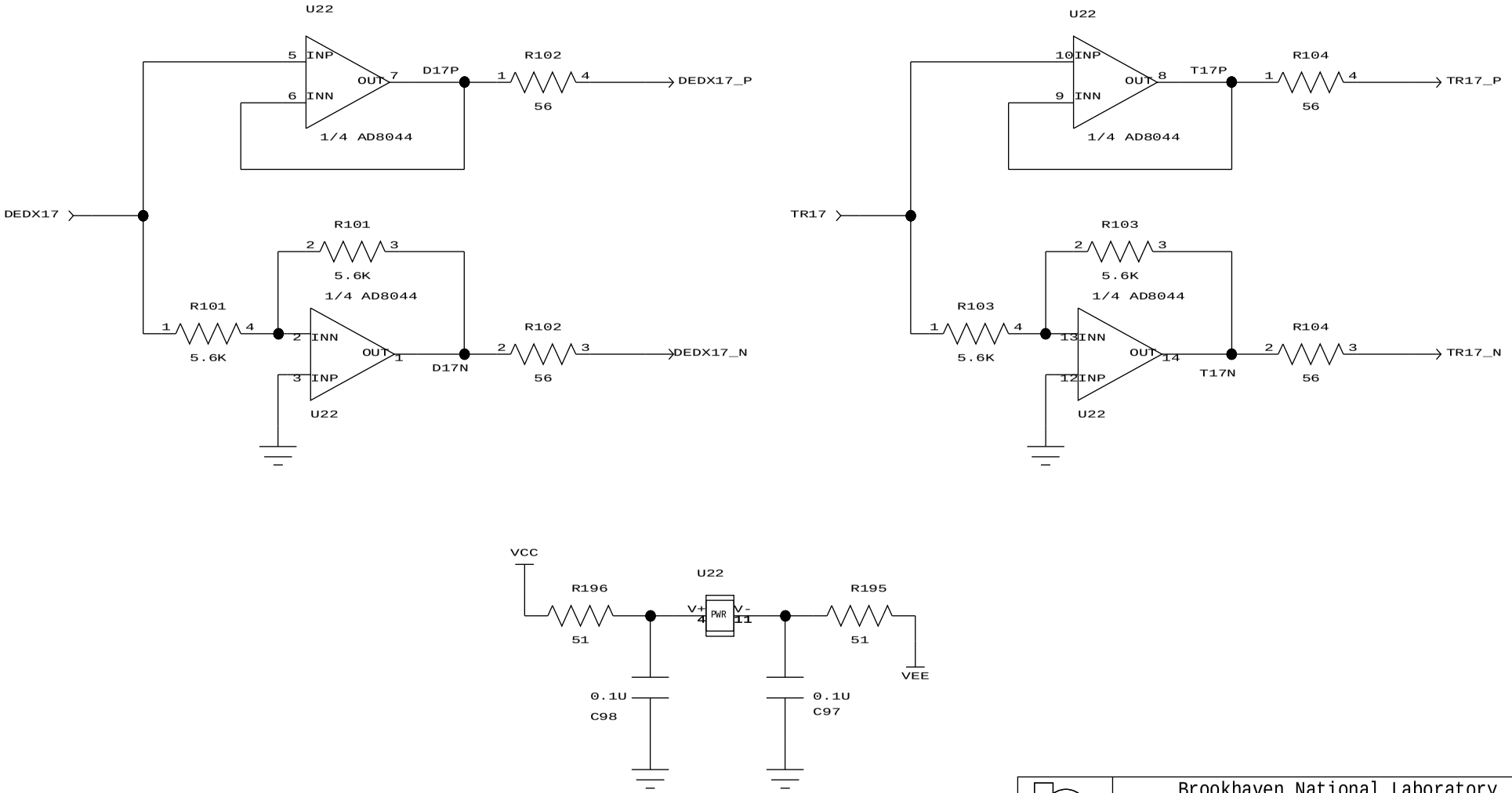

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Approvals	Date
Drawn	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 17; TR and dE/dX

Drawn By:
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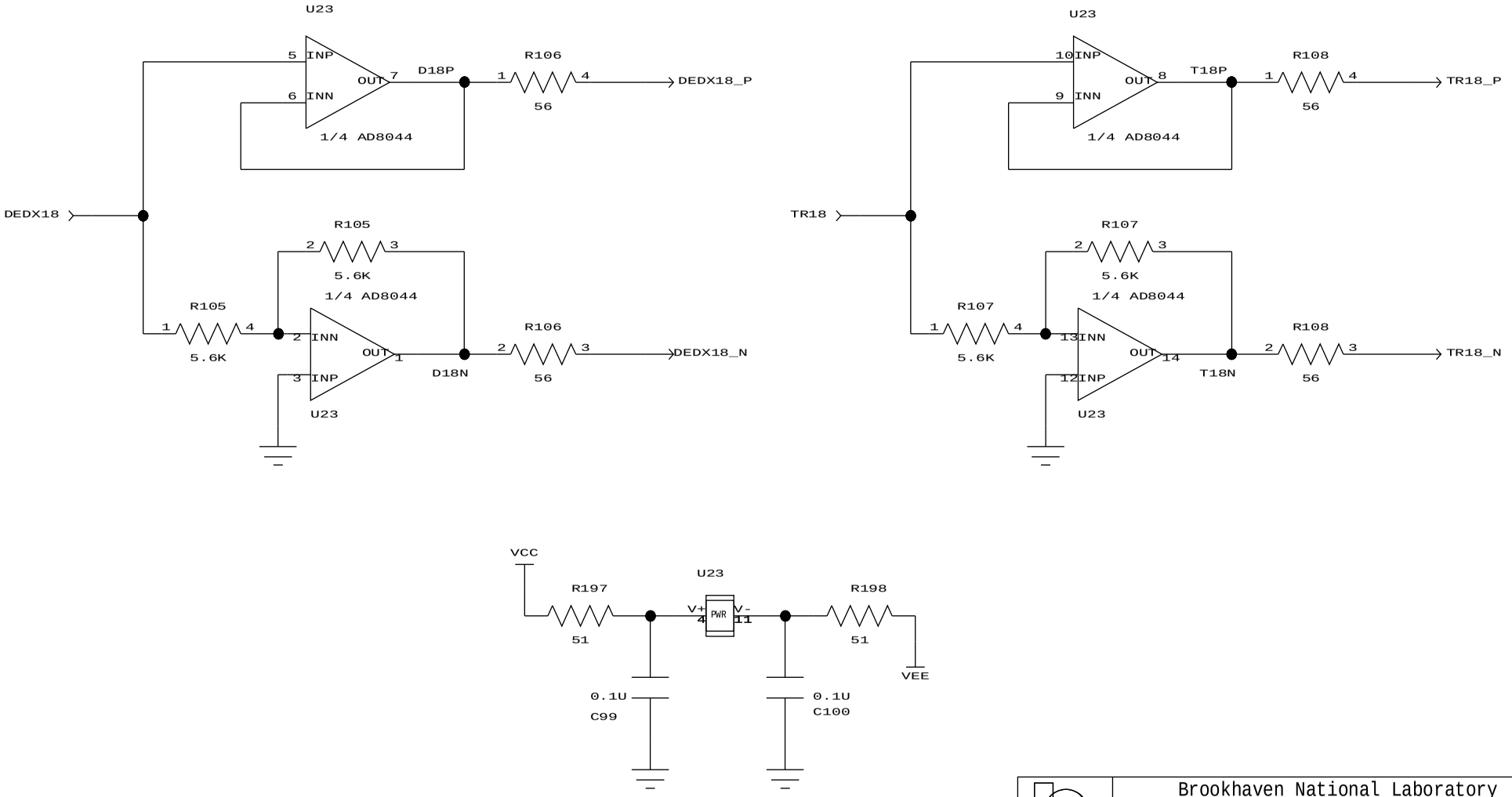

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 18; TR and dE/dX

Drawn By:
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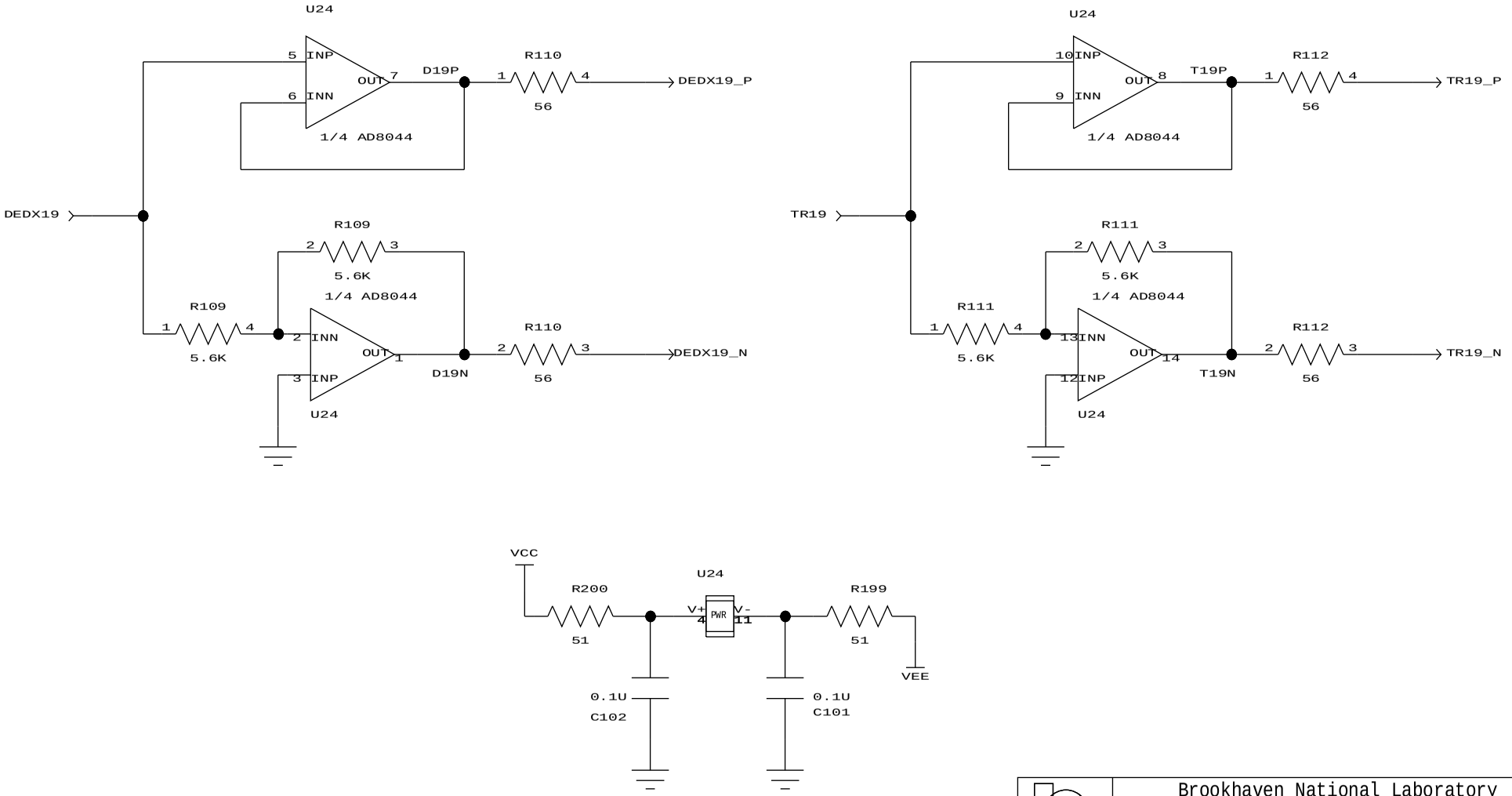

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@DATETIME=10-27-1997_13:00

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Upton, NY 11973

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 19; TR and dE/dX

Drawn By:
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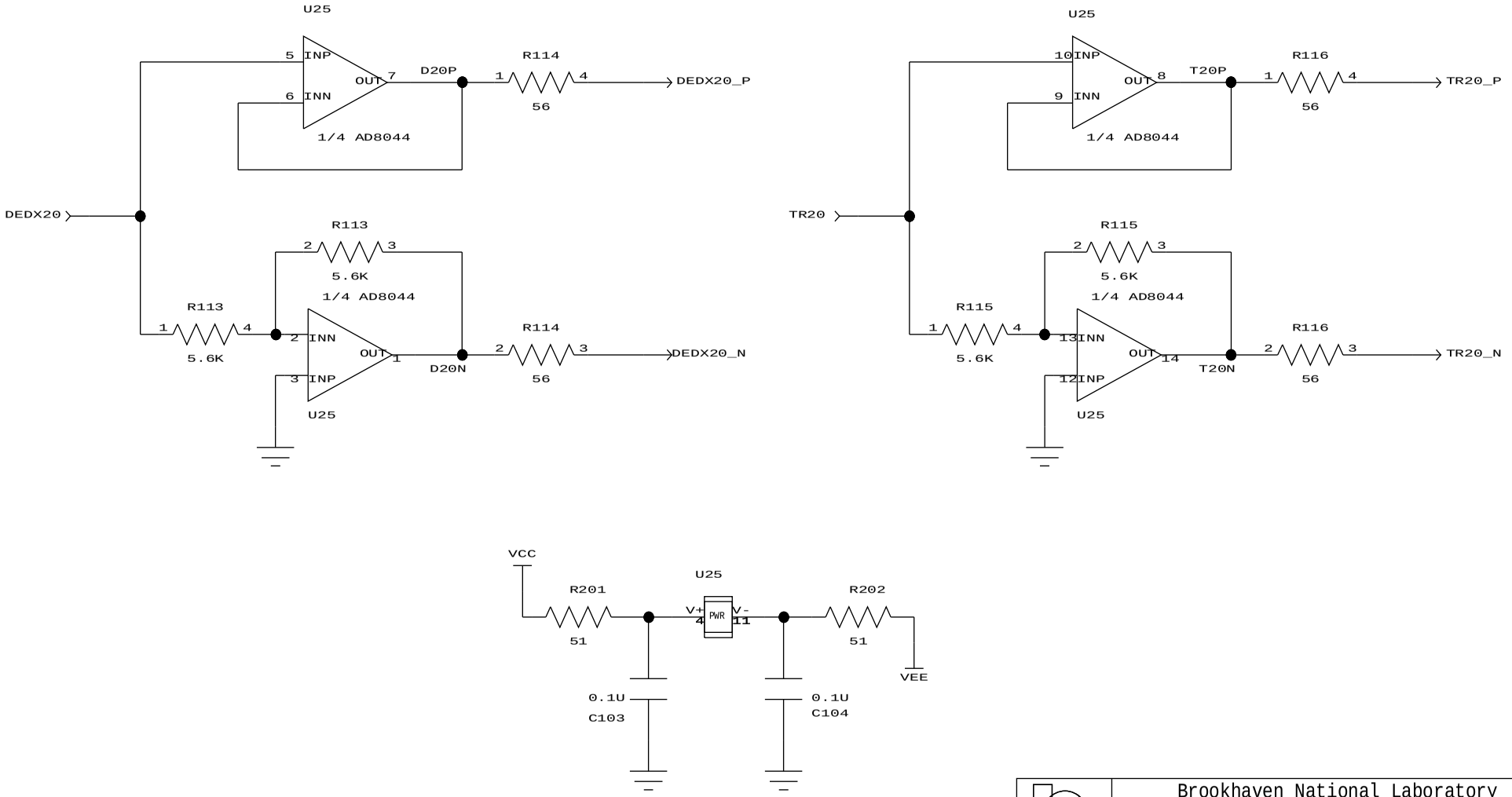

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Upton, NY 11973

Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 20; TR and dE/dX

Drawn By:
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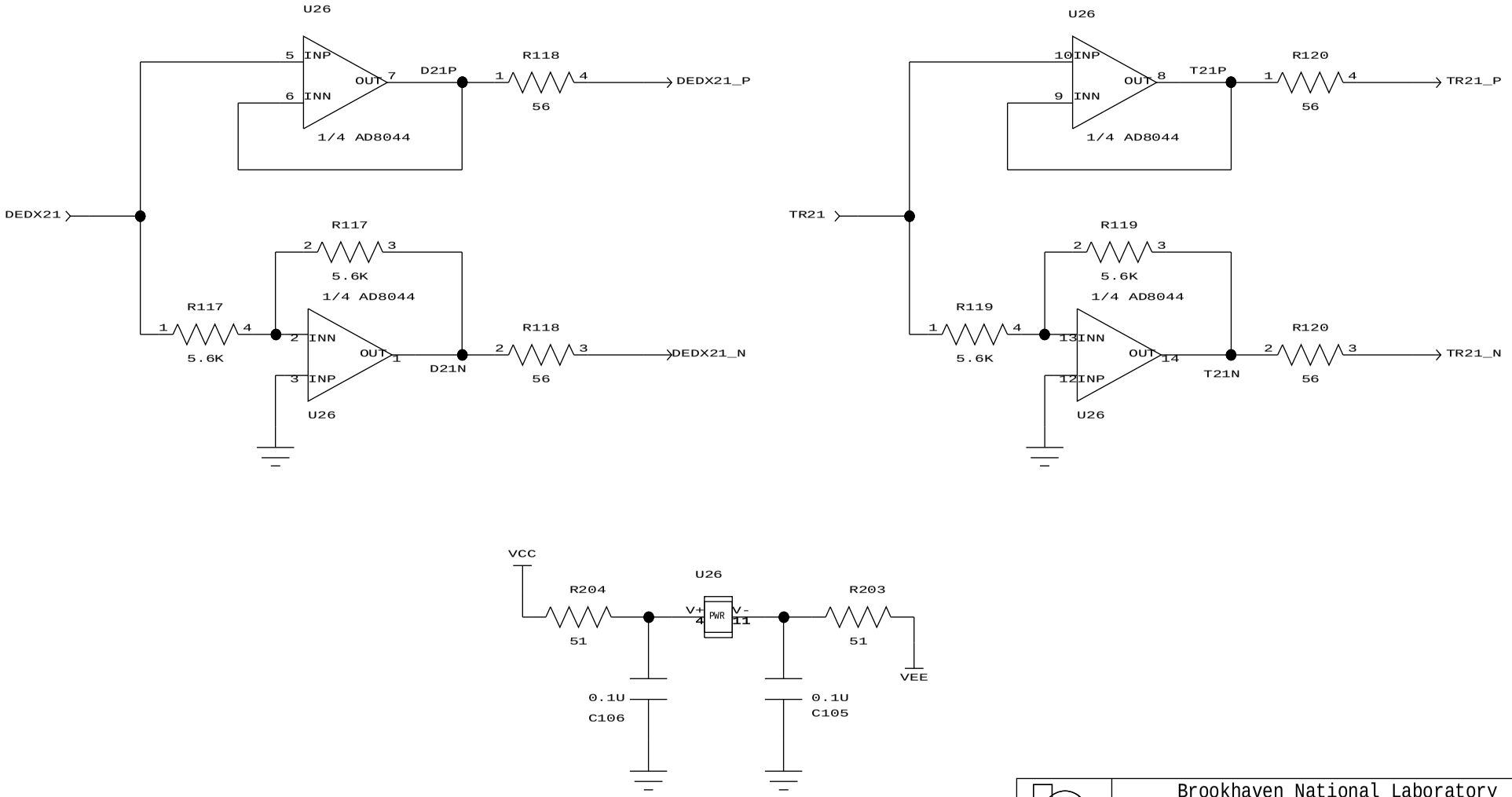

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 21; TR and dE/dX

Drawn By:
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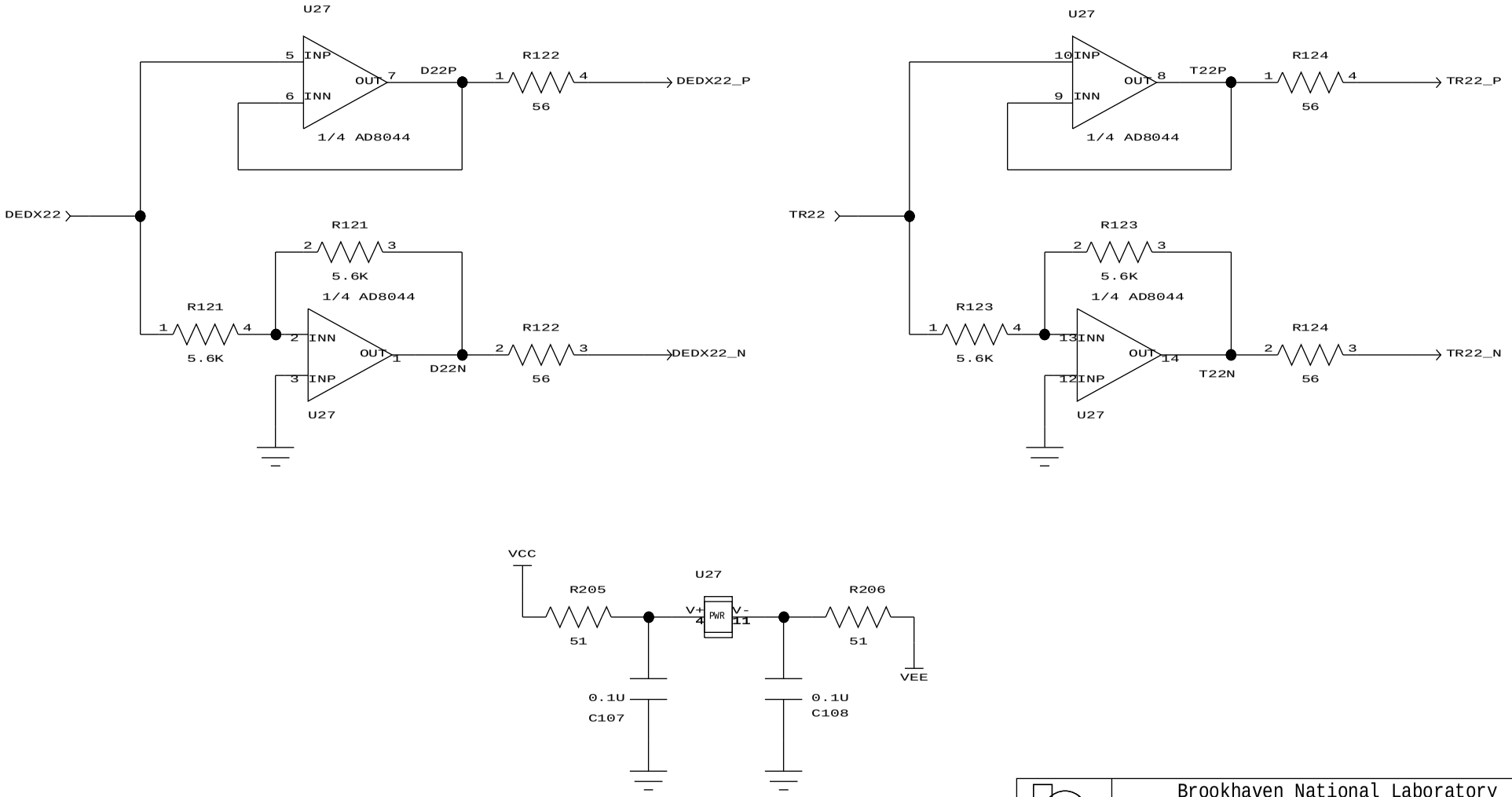

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Instrumentation Division
Upton, NY 11973

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Checked	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 22; TR and dE/dX

Drawn By:
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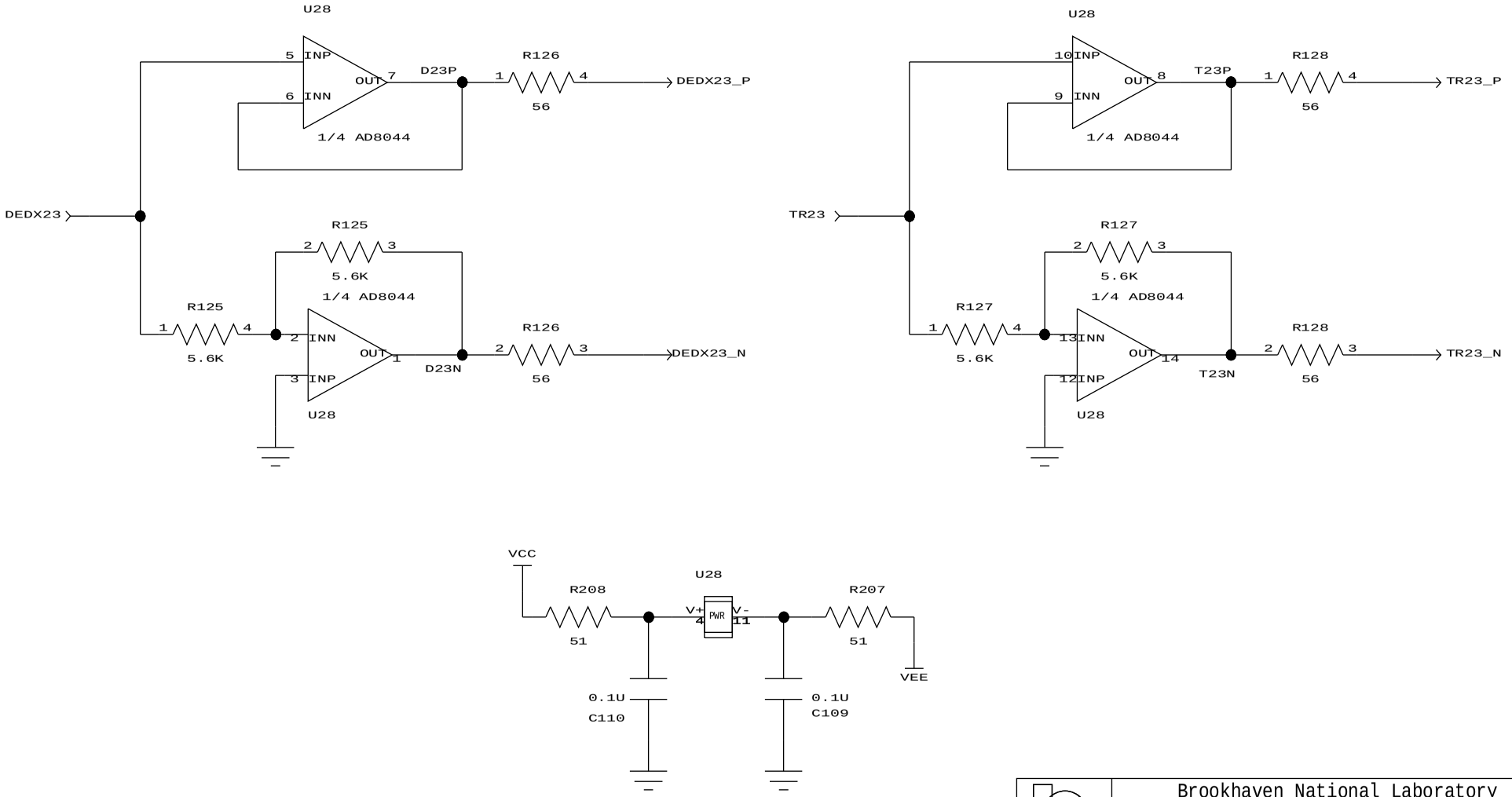

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Instrumentation Division
Upton, NY 11973

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Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 23; TR and dE/dX

Drawn By:
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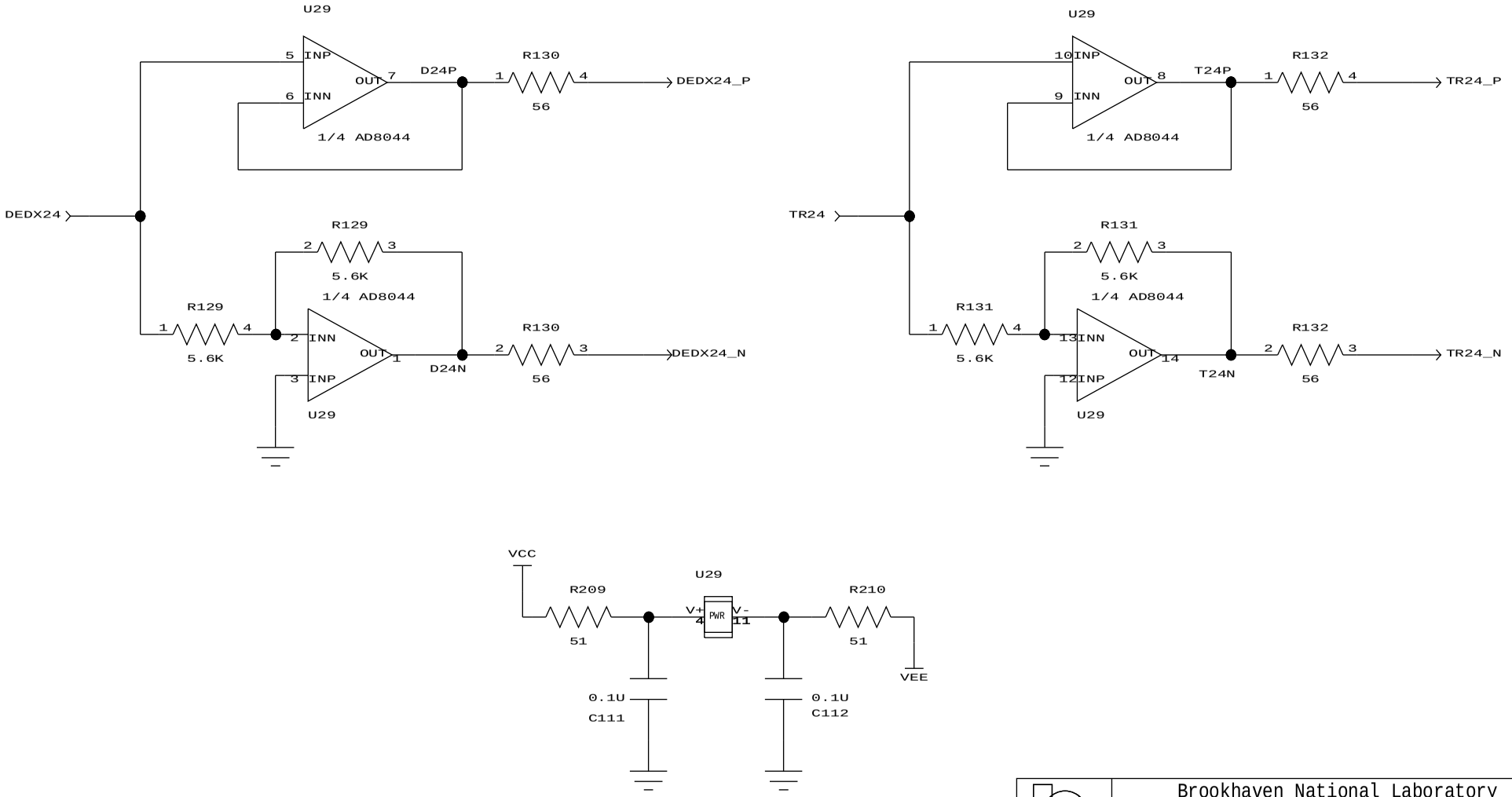

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Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 24; TR and dE/dX

Drawn By:
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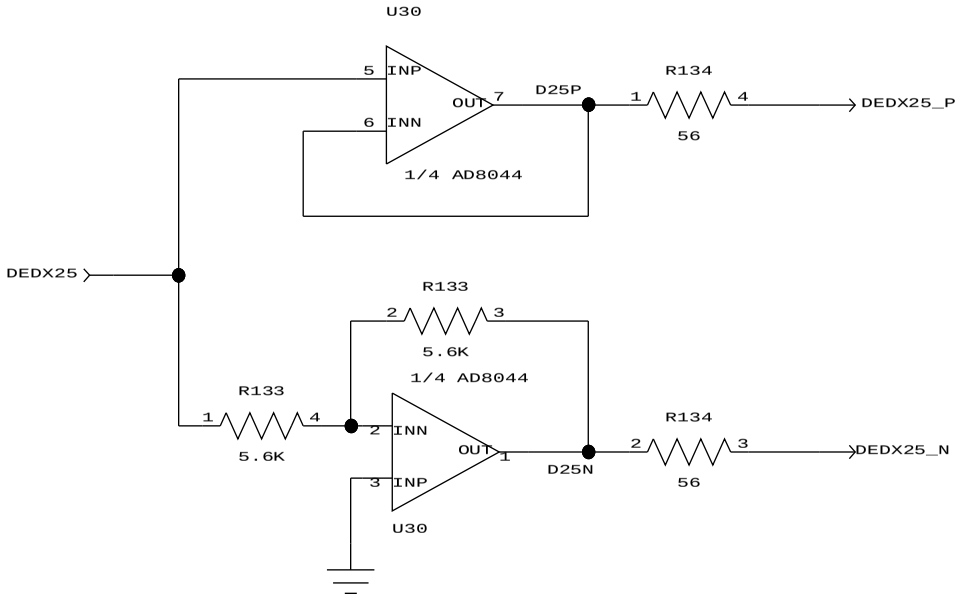

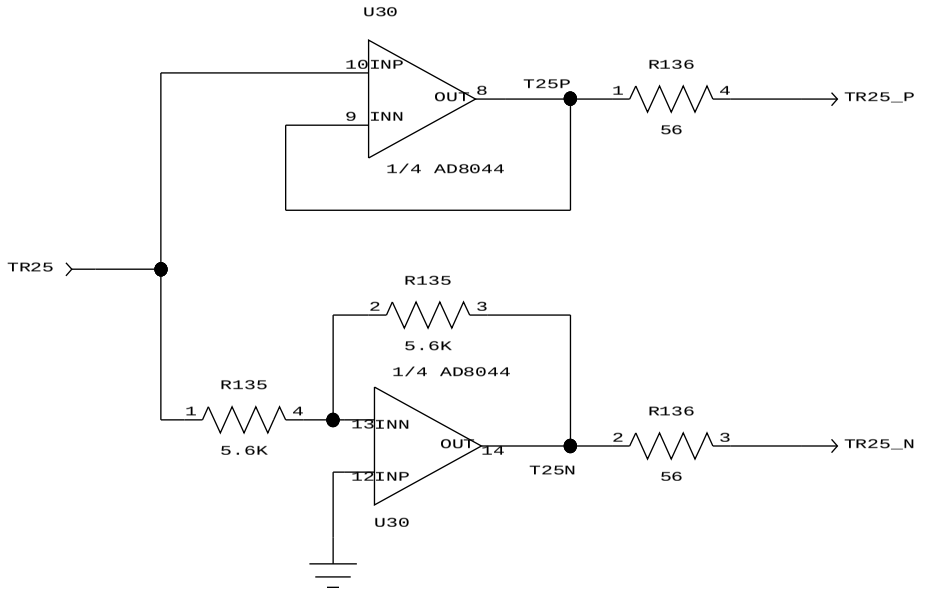

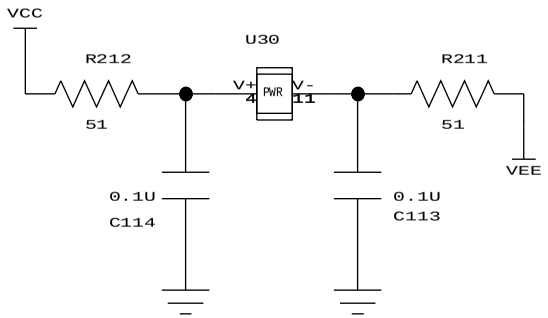

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@DATETIME=10-27-1997_13:01

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Instrumentation Division
Upton, NY 11973

Approvals	Date
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 25; TR and dE/dX

Drawn By:
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516-344-5486
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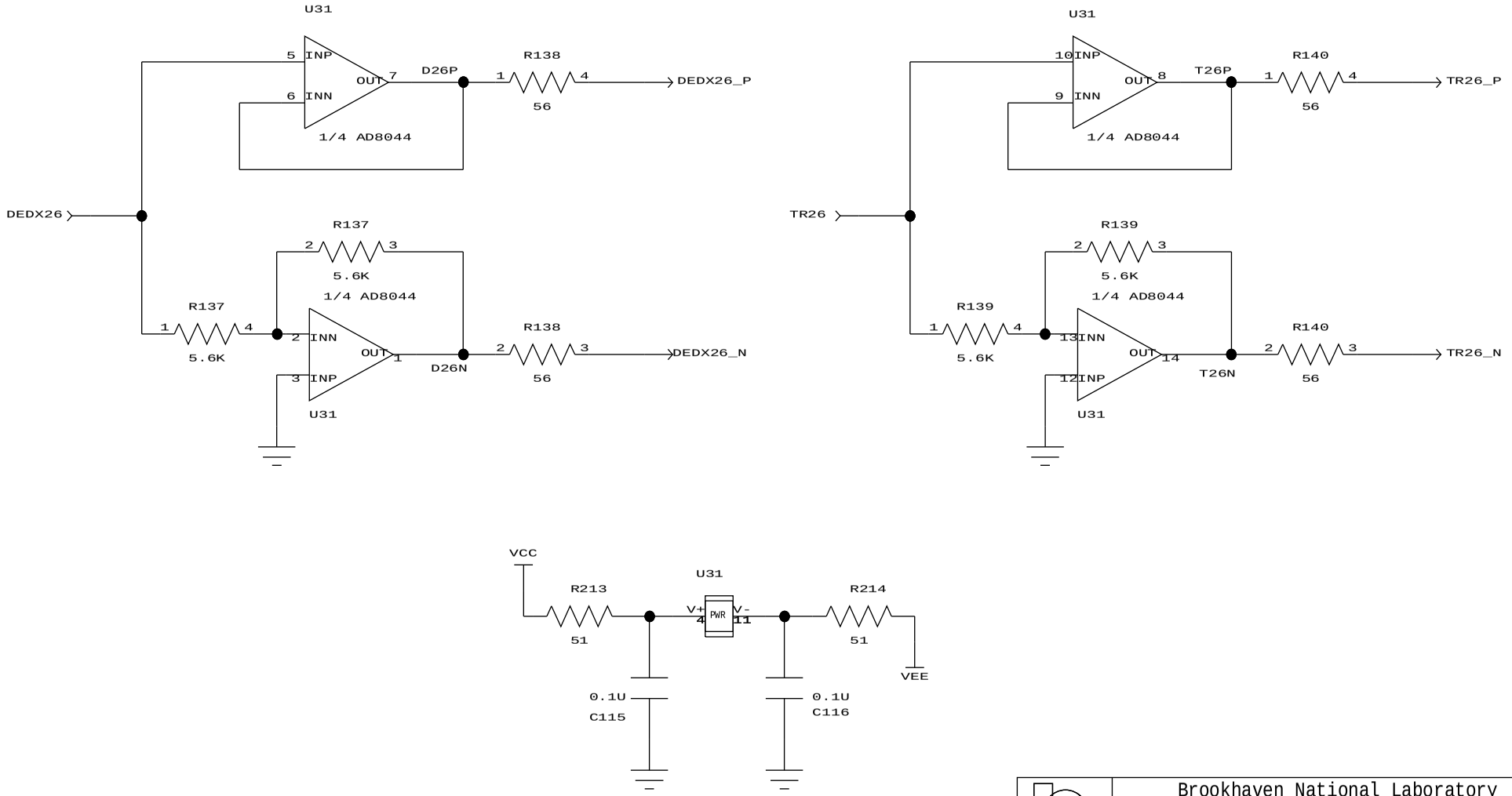

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@DATETIME=10-27-1997_13:01

Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
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Checked	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 26; TR and dE/dX

Drawn By:
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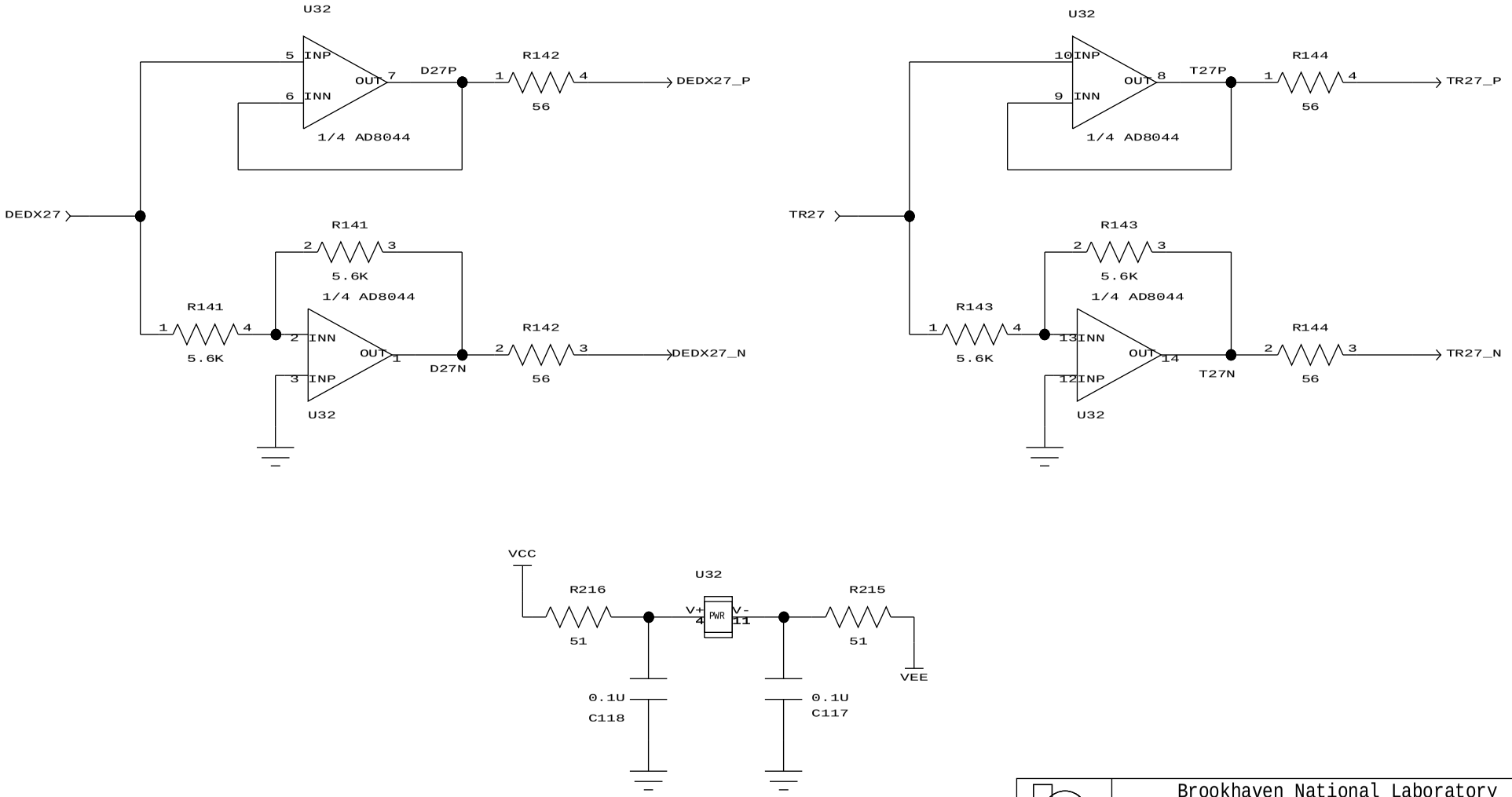

@NAME=tecps_r2a
@DATETIME=10-27-1997_13:01

Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 27; TR and dE/dX

Drawn By:
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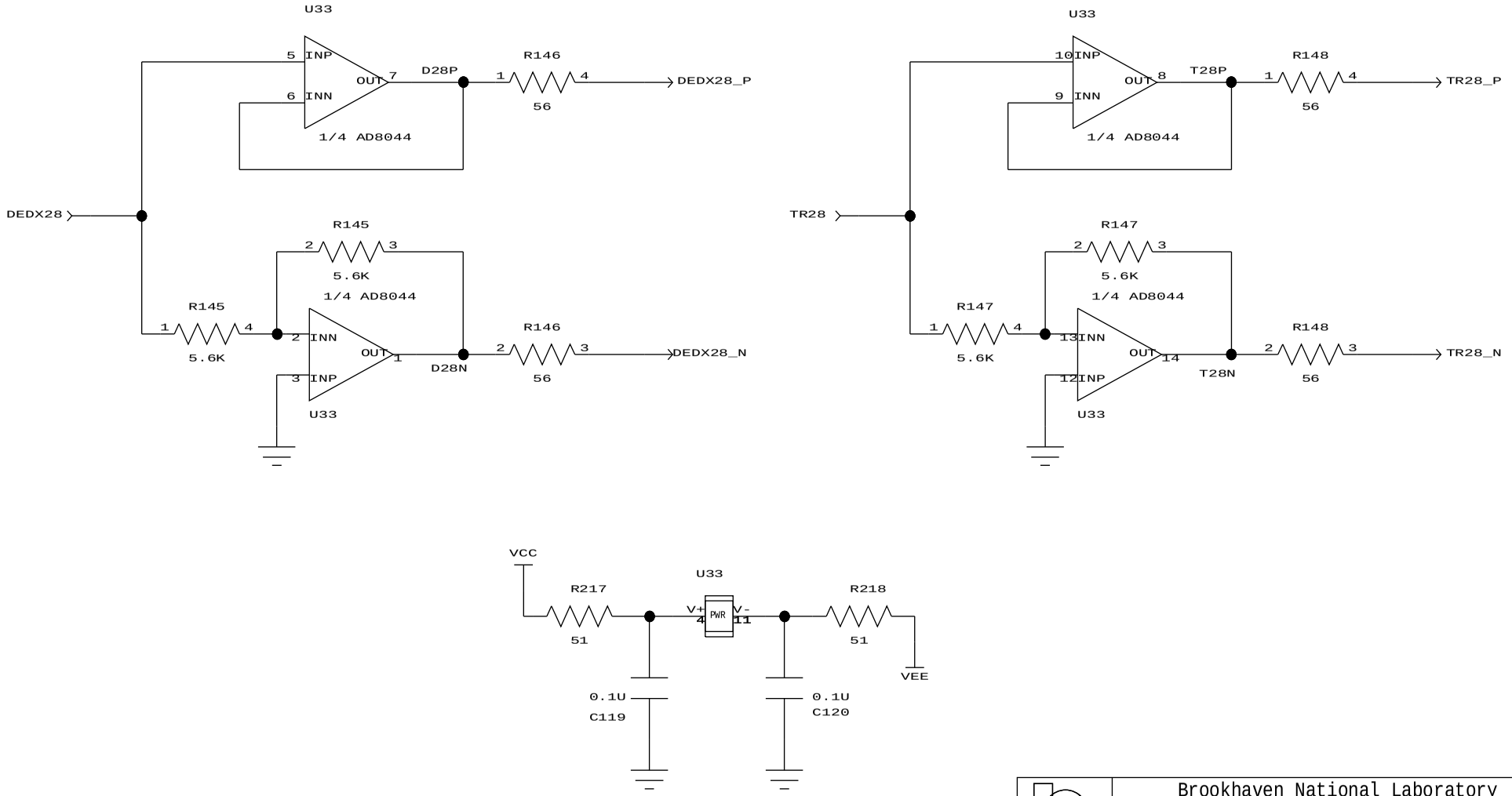
516-344-5486
anand@bnl.gov



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@DATETIME=10-27-1997_13:01

Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 28; TR and dE/dX

Drawn By:
Anand Kandasamy
516-344-5486
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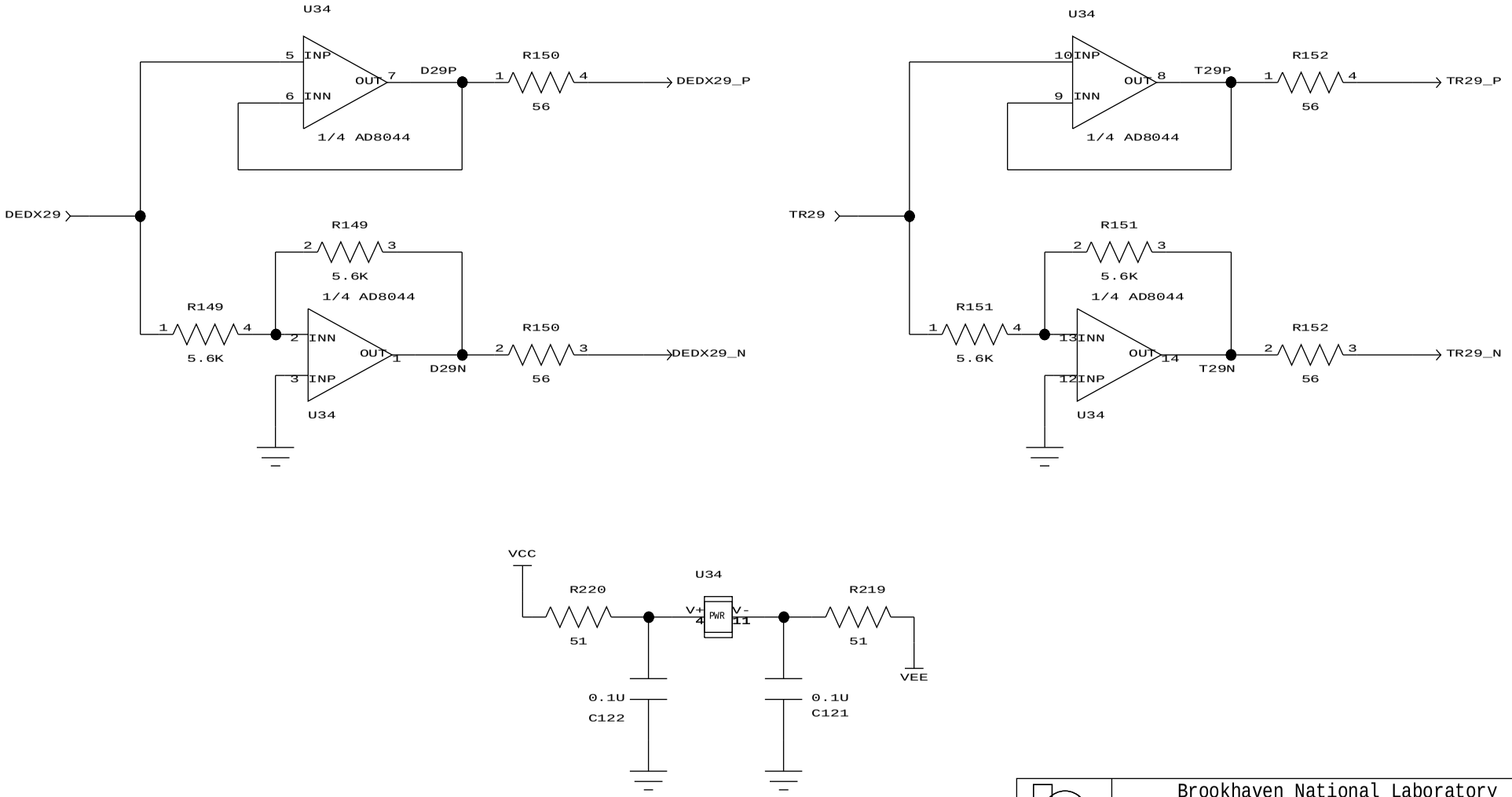

@NAME=tecps_r2a
@DATETIME=10-27-1997_13:01

Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 29; TR and dE/dX

Drawn By:
Anand Kandasamy
516-344-5486
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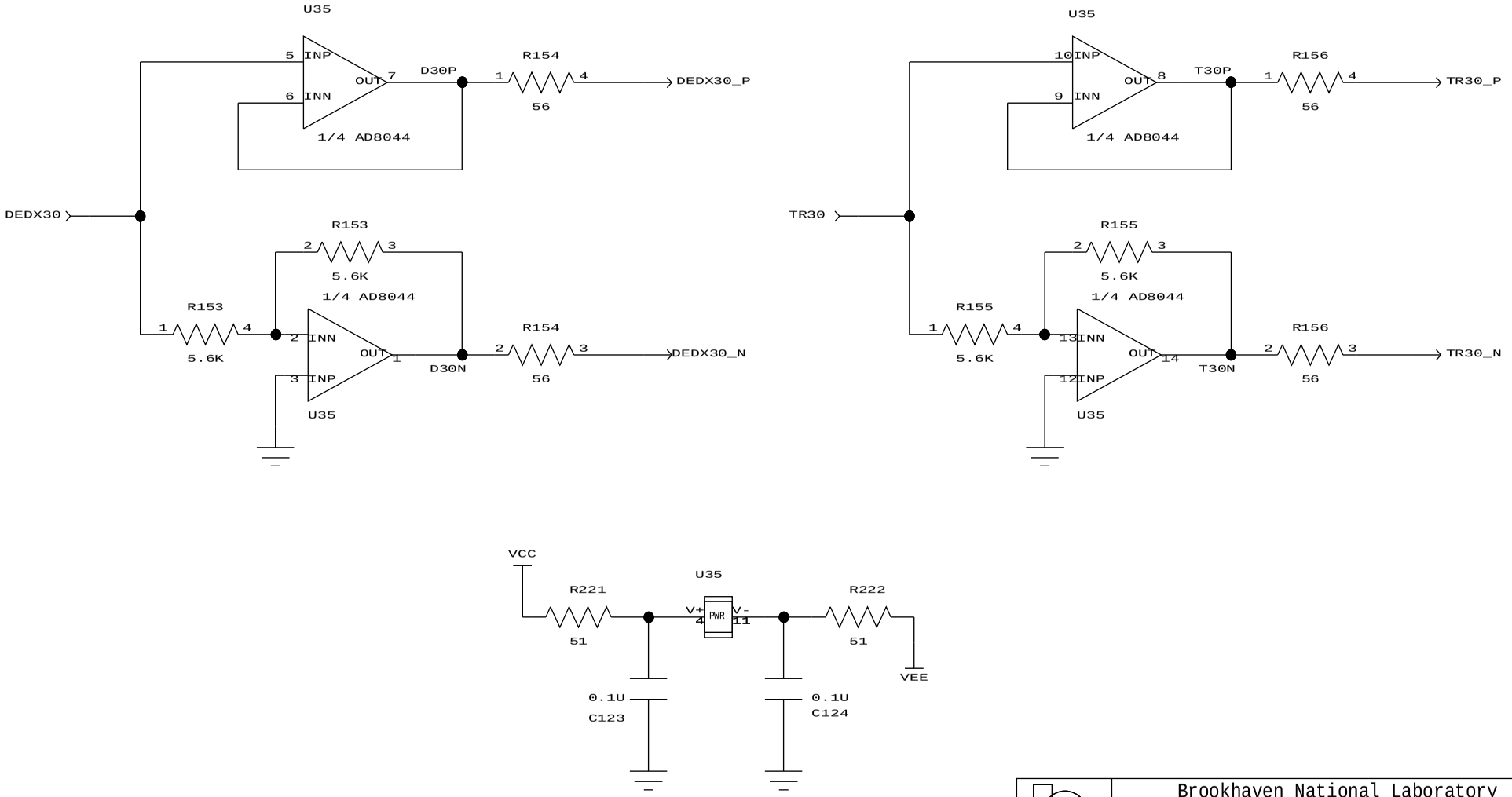

@NAME=tecps_r2a
@DATETIME=10-27-1997_13:01

Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 30; TR and dE/dX

Drawn By:
Anand Kandasamy
516-344-5486
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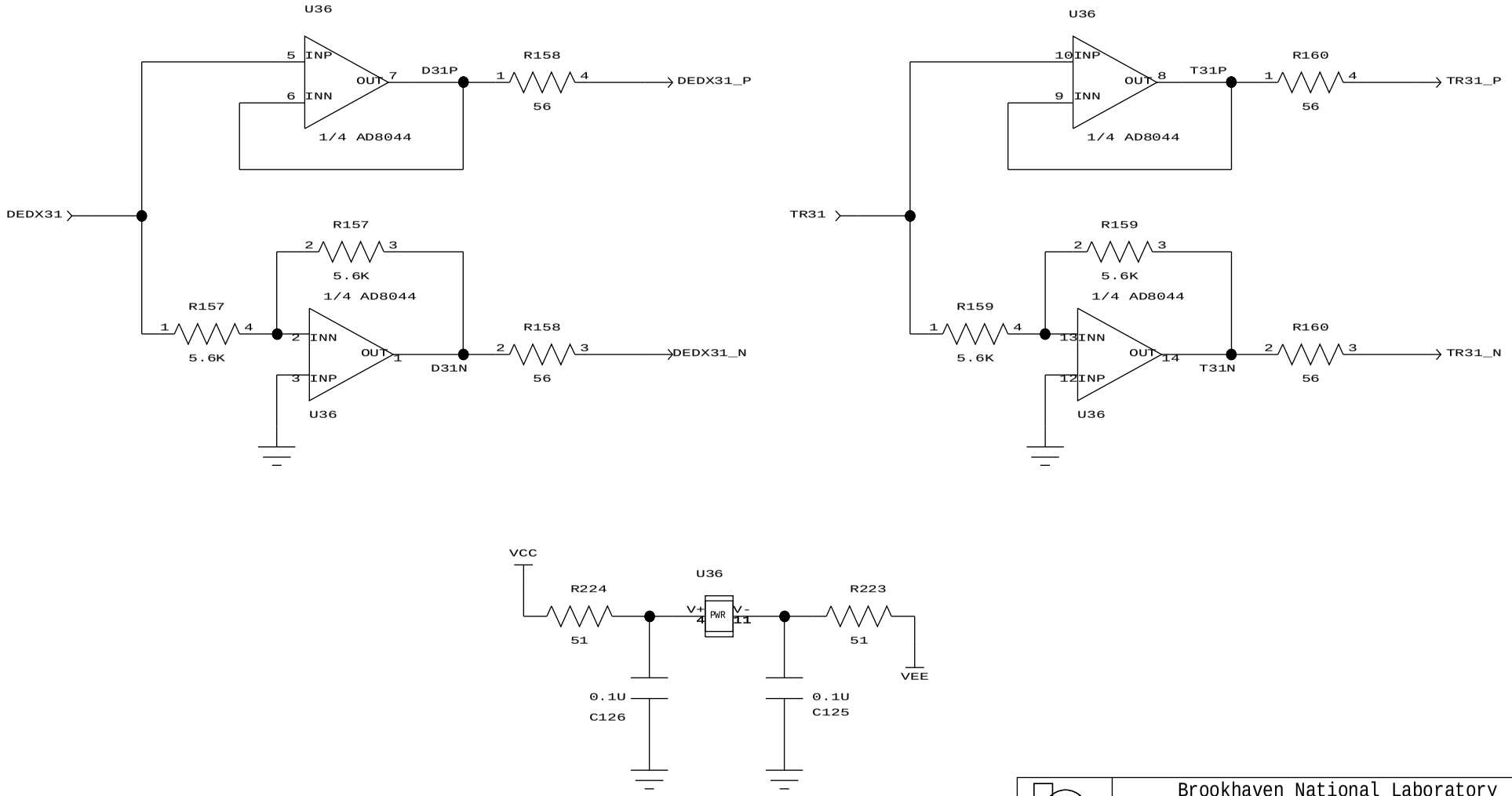

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@DATETIME=10-27-1997_13:01

Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
Channel 31; TR and dE/dX

Drawn By:
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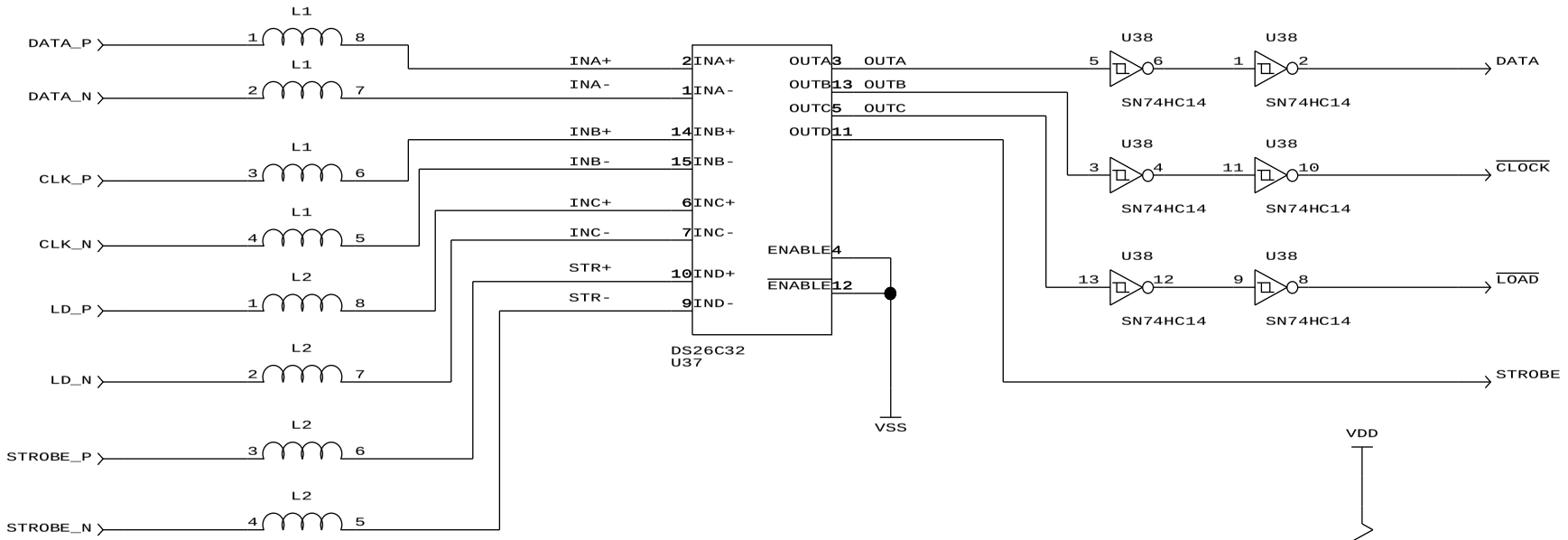
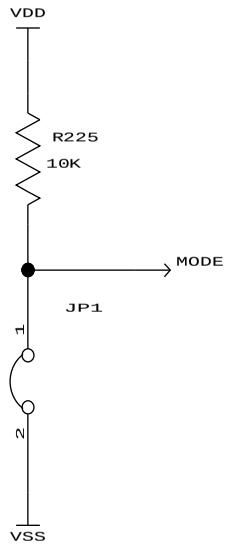
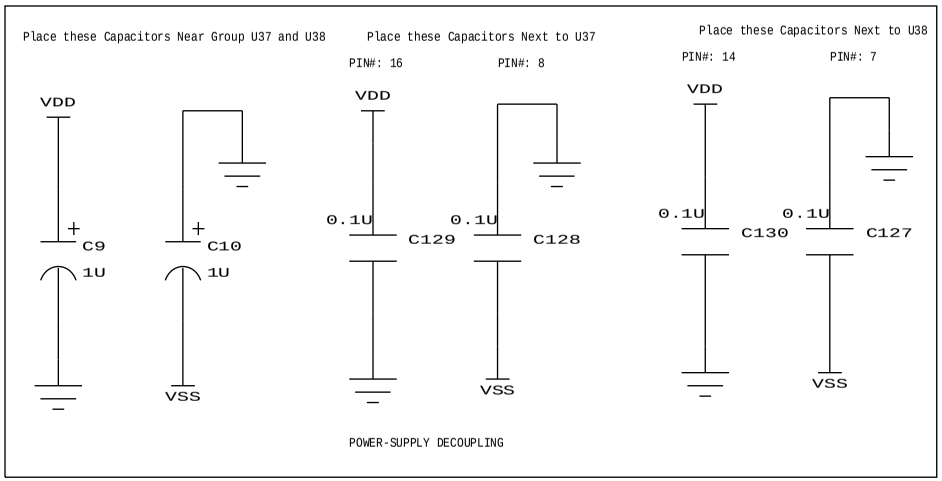




POWER U37		
PIN#: 16	VDD	+2.5V
PIN#: 8	VSS	-2.5V

POWER U38		
PIN#: 14	VDD	+2.5V
PIN#: 7	VSS	-2.5V



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Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
RS-422 Serial Link Receivers

Drawn By:
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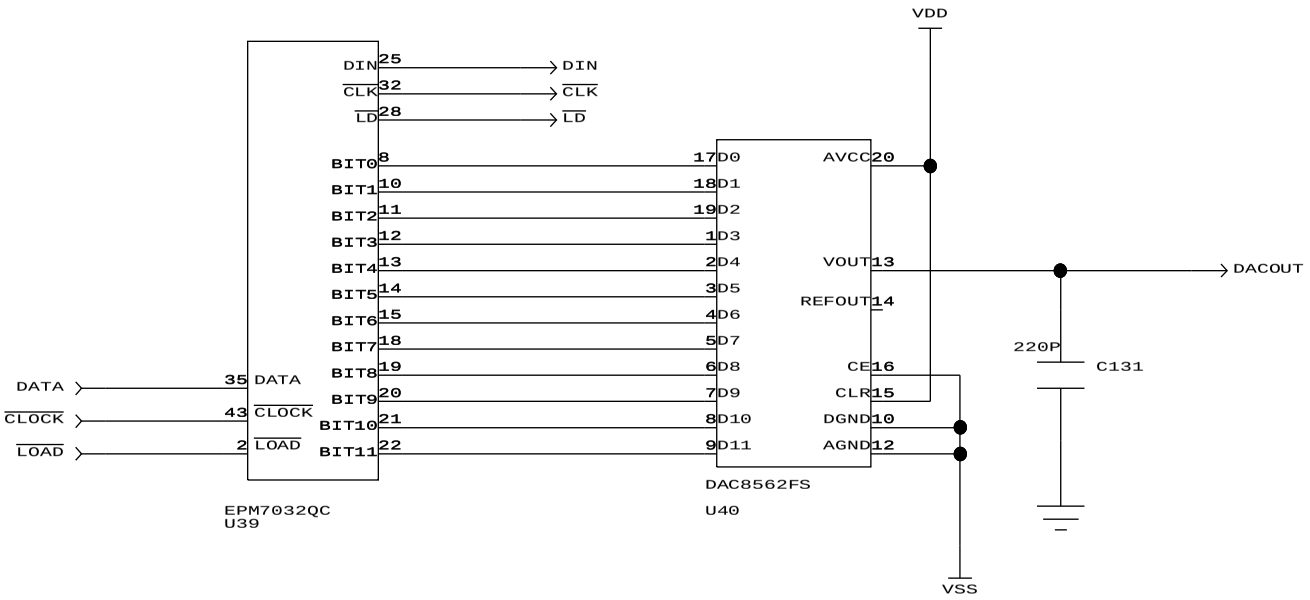
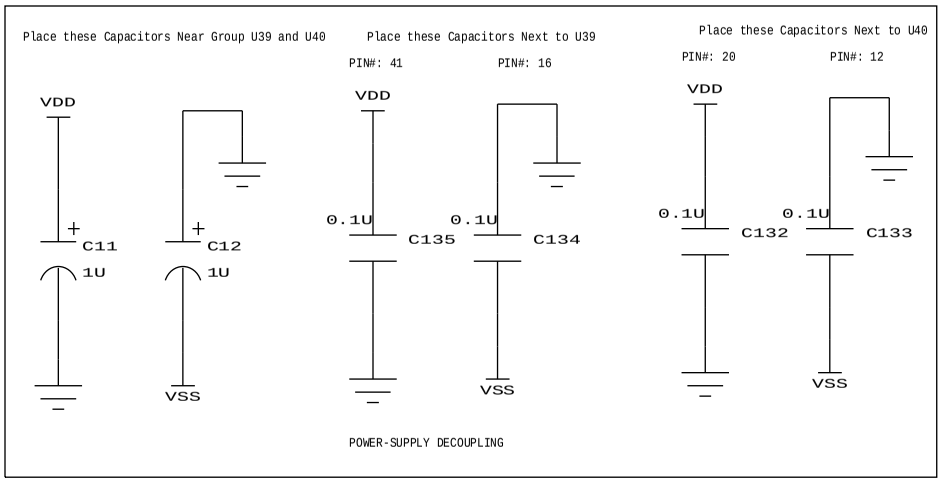
516-344-5486
anand@bnl.gov



POWER U39		
PIN#: 9,17,29,41	VDD	+2.5V
PIN#: 4,16,24,36,37,38,39,40	VSS	-2.5V



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Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
Drawn	
Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
EPLD and DAC

Drawn By:
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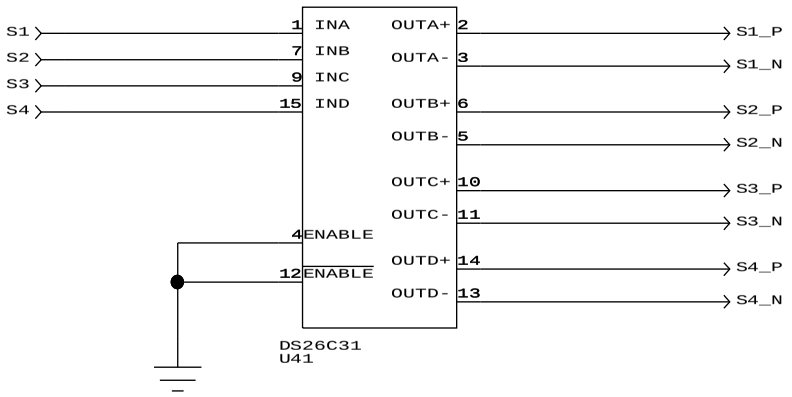
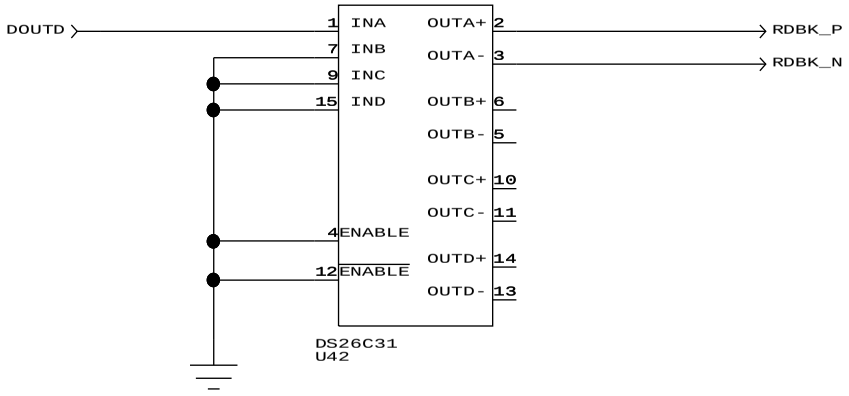
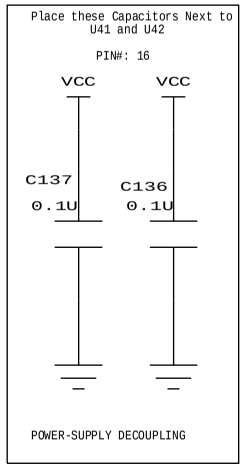




POWER U41 and U42		
PIN#: 16	VCC	+5V
PIN#: 8	GND	0V



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Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973

Approvals	Date
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Checked	
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Drawing:

PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels

Address bit and Readback

Drawn By:
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516-344-5486
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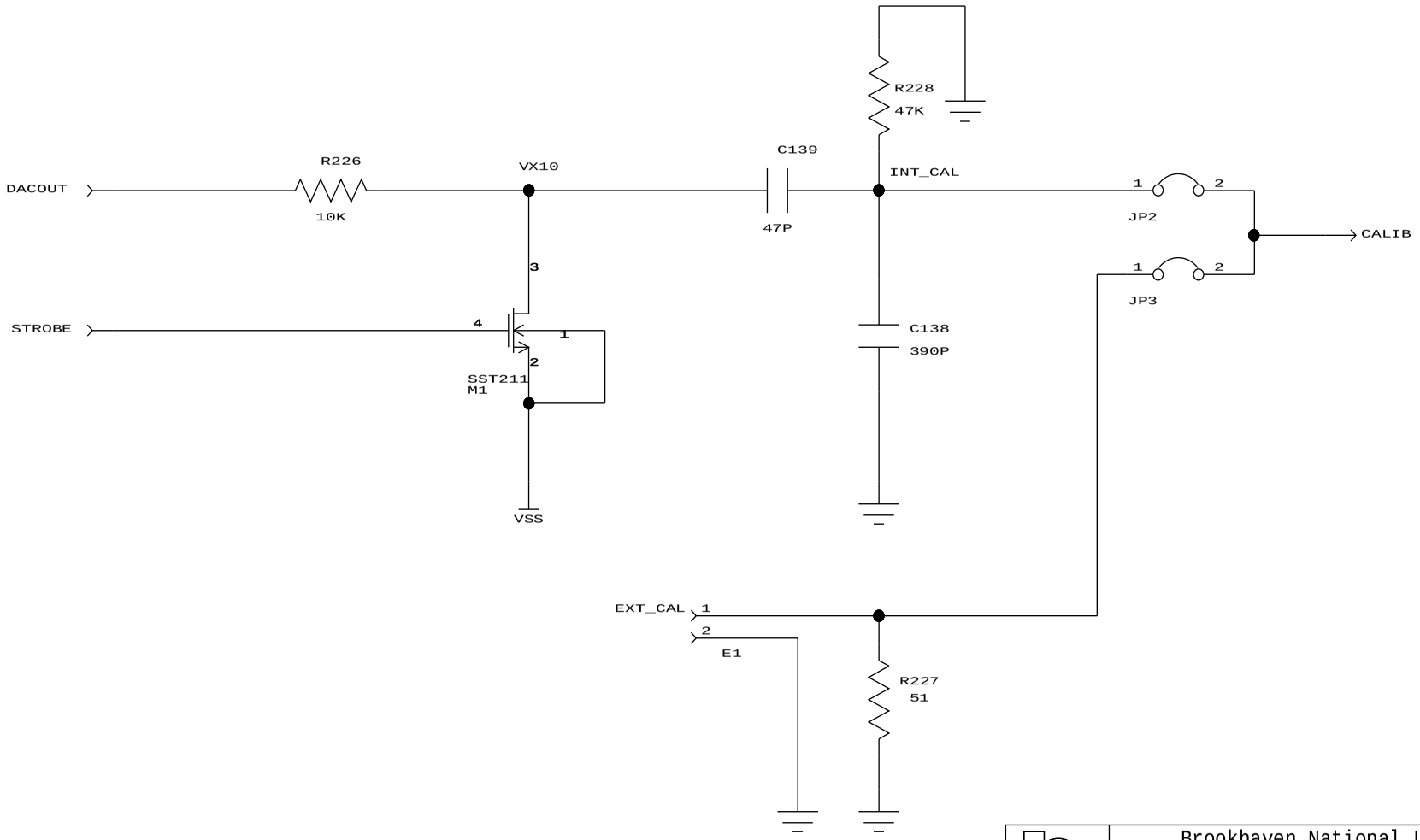
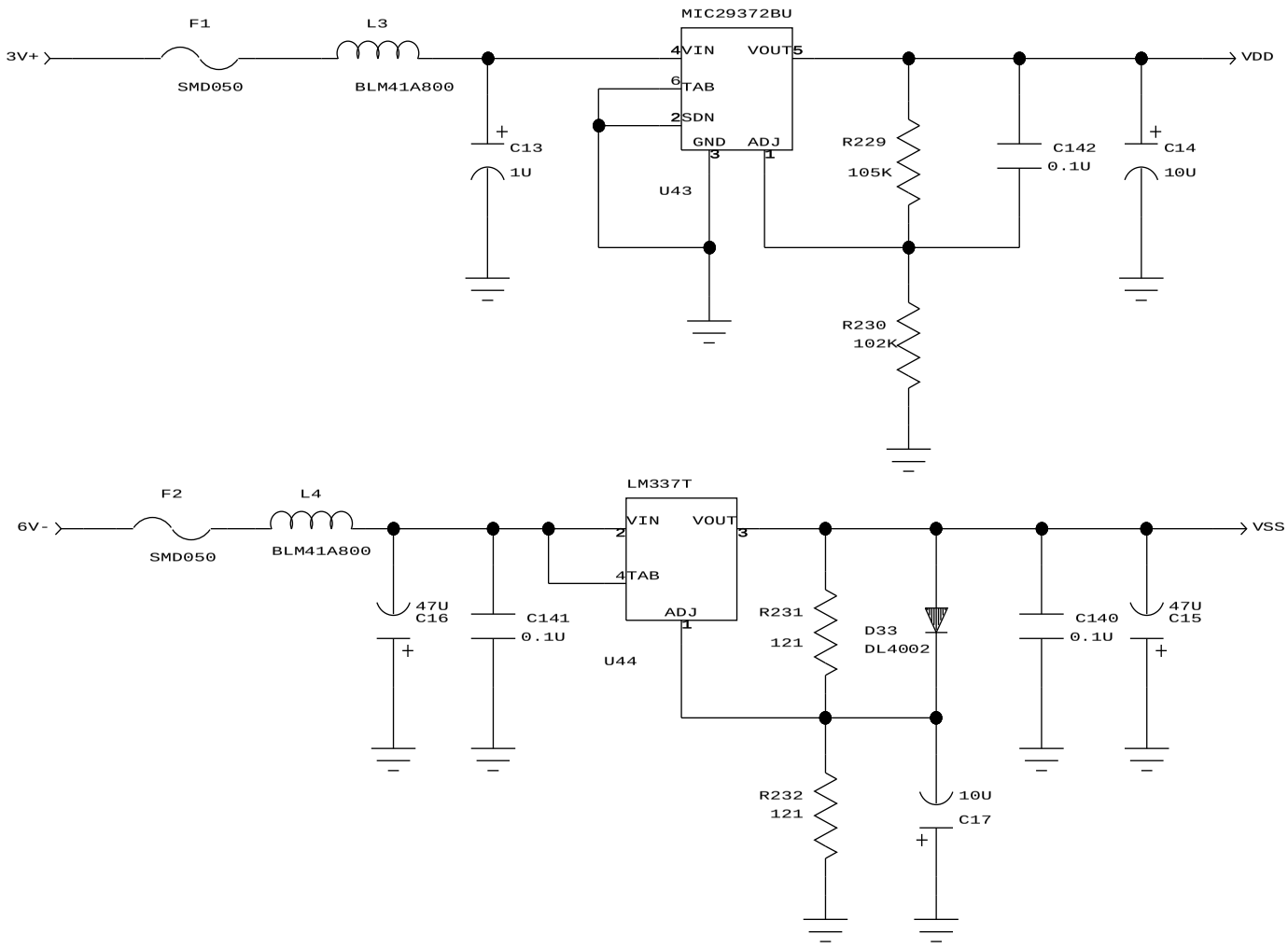


Brookhaven National Laboratory Instrumentation Division Upton, NY 11973	
Approvals / Date	Drawing: PHENIX Time Expansion Chamber Preamp-Shaper Front End Electronics
Drawn	
Checked	
Issued	
SIZE: B DWG NO: REV NO: 1 SCALE	TECPS Rev2 - 32 Channels Internal Calibration Circuit
Drawn By: Anand Kandasamy 516-344-5486 anand@bnl.gov	Sheet: 40 of 46

@NAME=tecps_r2a
@DATETIME=10-27-1997_13:01



POWER SUPPLY REGULATION		
Unregulated Supply	Regulated Supply	Voltage
+3V	VDD	+2.5V
+6V	VCC	+5.0V
-6V	VEE	-5.0V
-6V	VSS	-2.5V

@NAME=tecps_r2a
@DATETIME=8-25-1997_15:29

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
+2.5V and -2.5V Voltage Regulators

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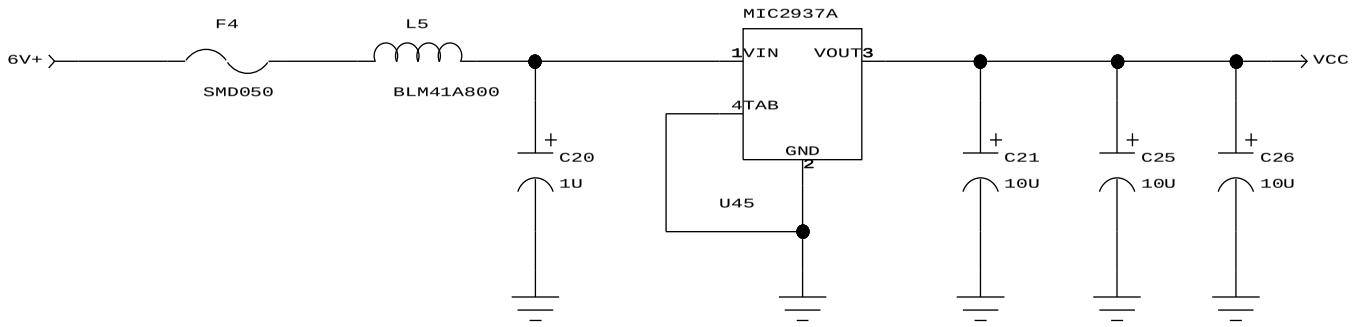

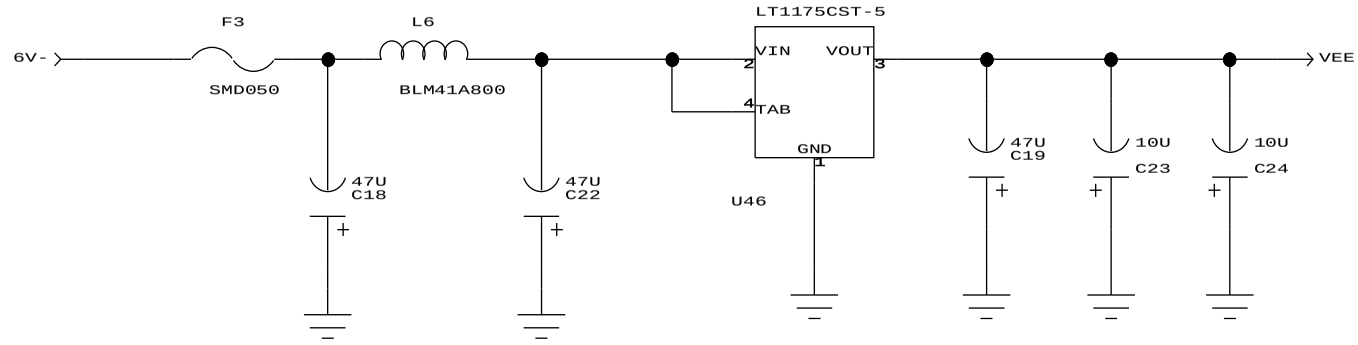

POWER SUPPLY REGULATION		
Unregulated Supply	Regulated Supply	Voltage
+3V	VDD	+2.5V
+6V	VCC	+5.0V
-6V	VEE	-5.0V
-6V	VSS	-2.5V

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@DATETIME=8-21-1997_8:44

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Approvals	Date
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Checked	
Issued	

Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
+5.0V and -5.0V Voltage Regulators

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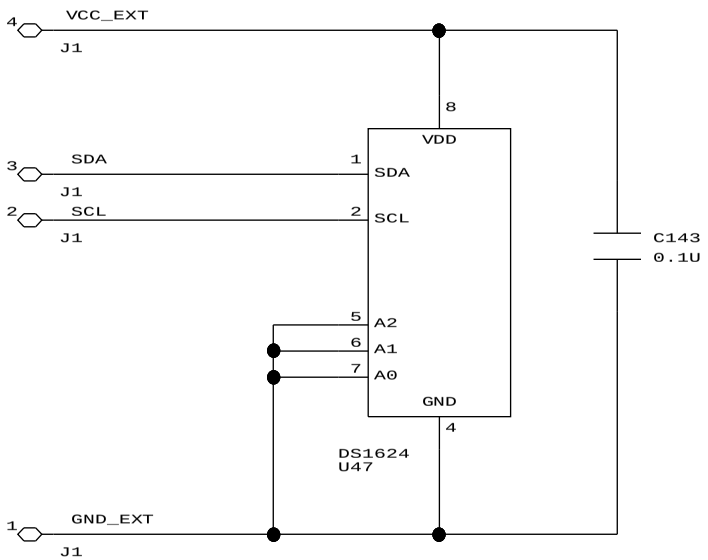

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Approvals	Date
Drawn	
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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels

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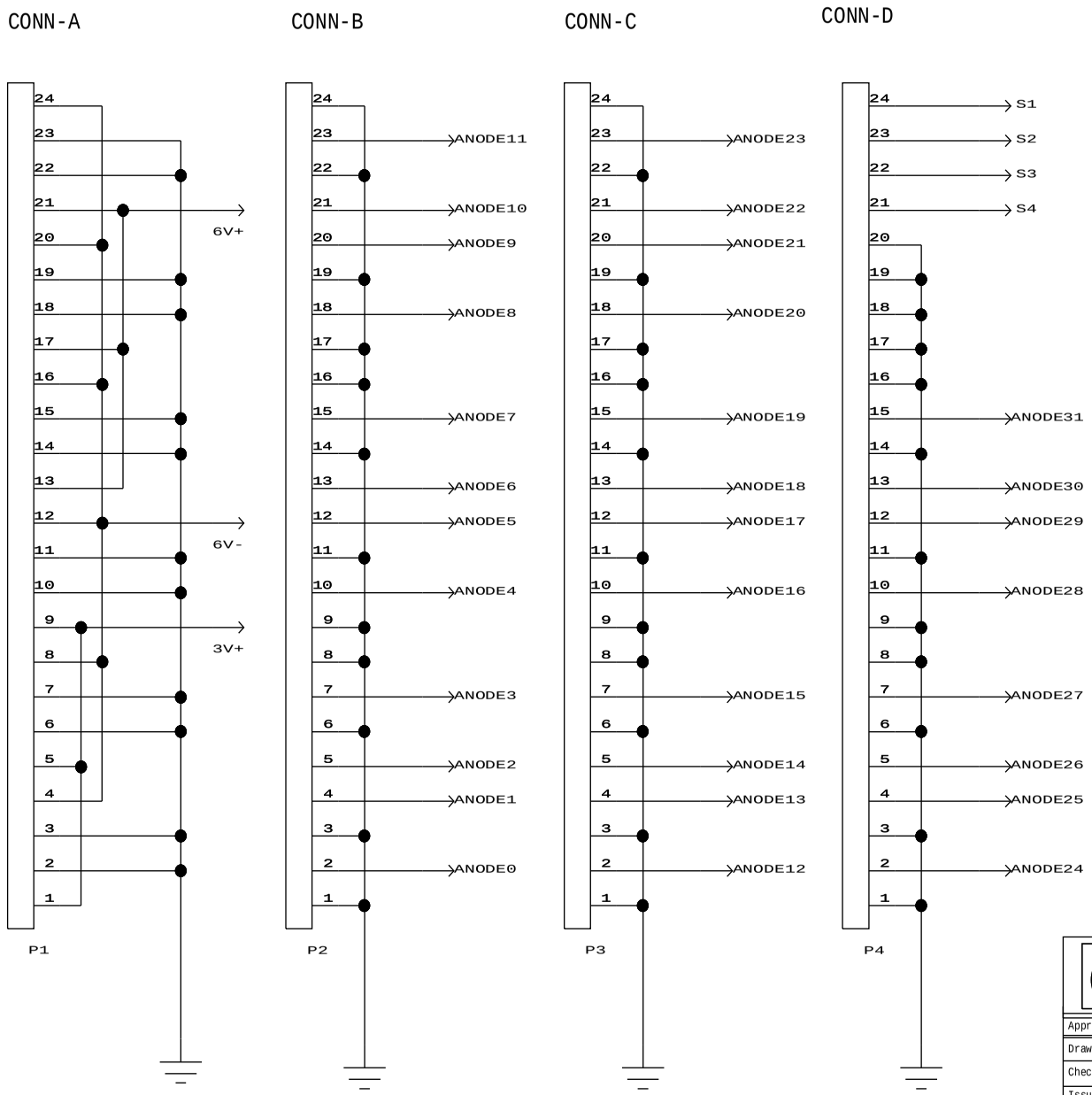

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Approvals	Date
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Drawing:

PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels

ANODE BOARD interface connectors

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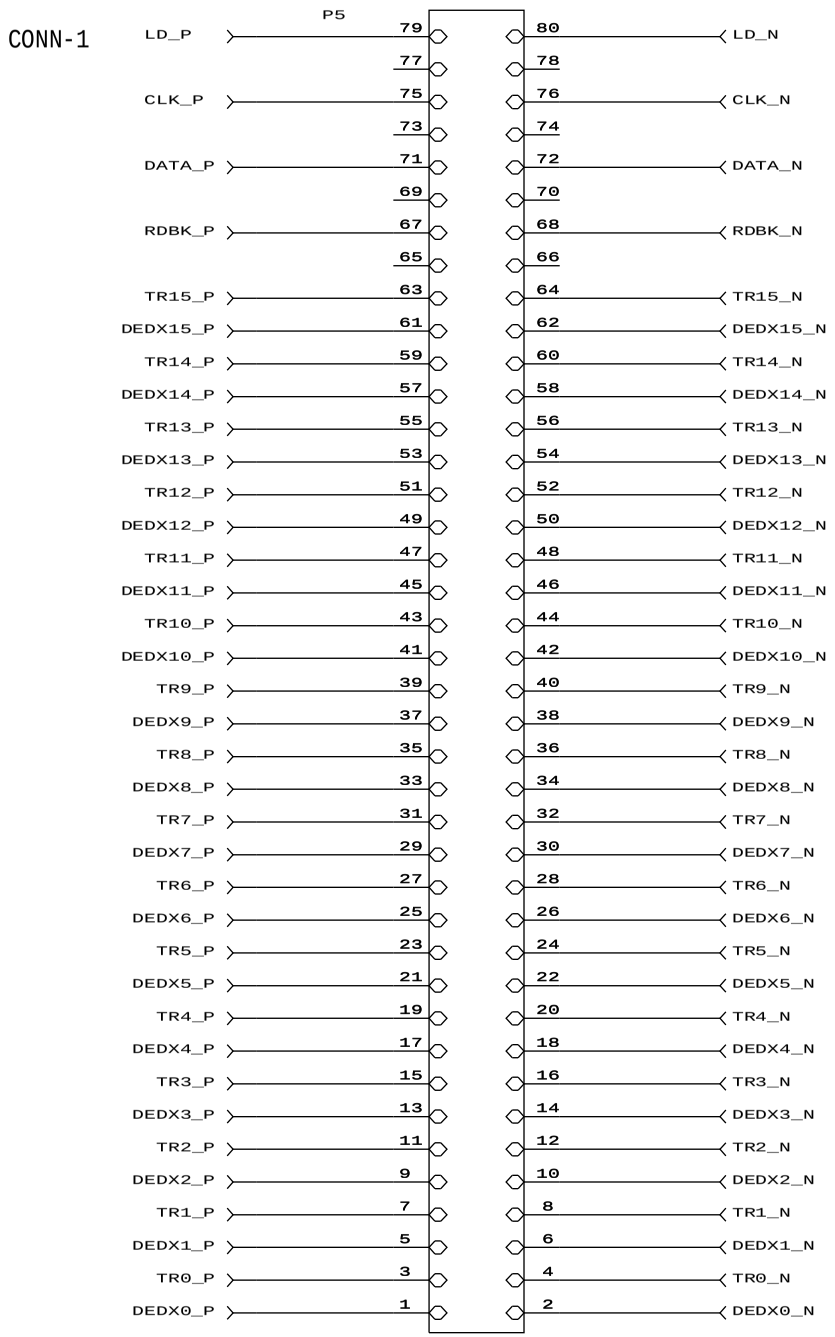

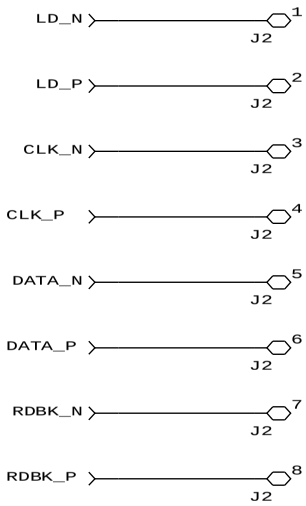

CONN-3

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@DATETIME=10-27-1997_13:04

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Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

TECPS Rev2 - 32 Channels
FEM Interface Connector and Serial Connector

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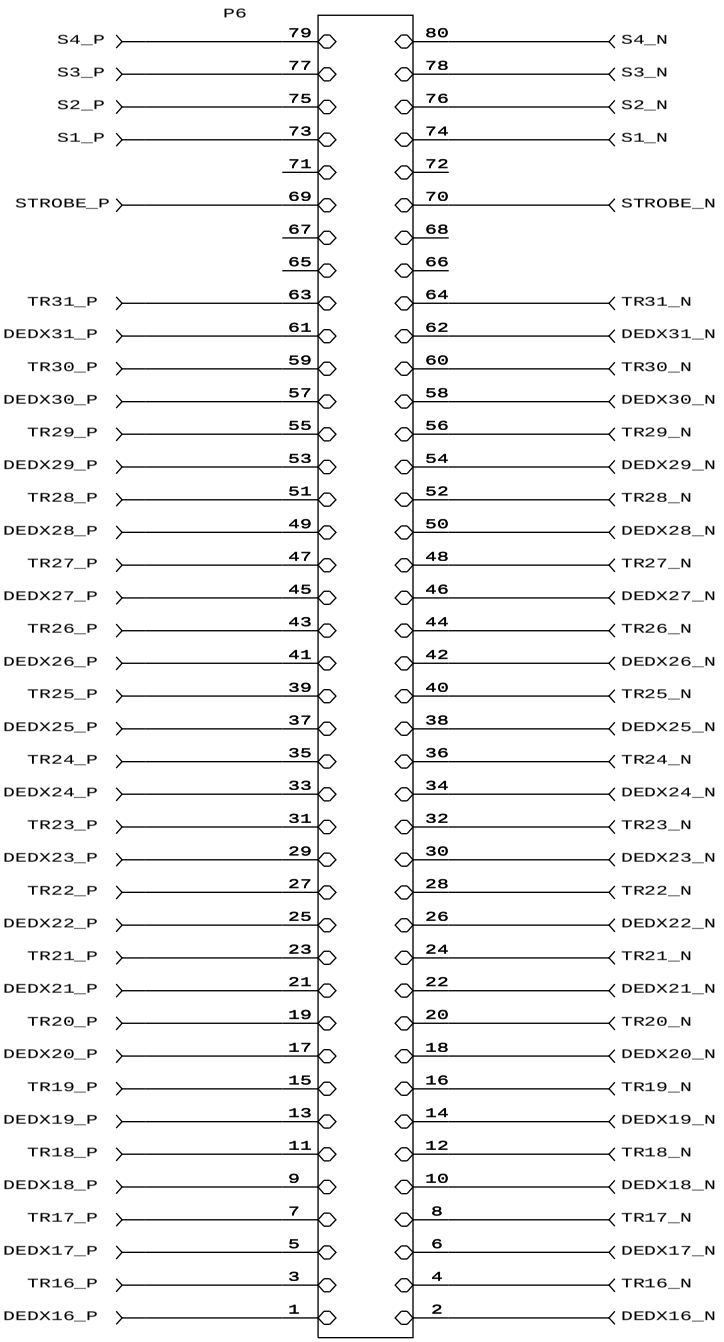
CONN-2
P6
S4_P 79
S3_P 77
S2_P 75
S1_P 73
71
STROBE_P 69
67
65
TR31_P 63
DEDX31_P 61
TR30_P 59
DEDX30_P 57
TR29_P 55
DEDX29_P 53
TR28_P 51
DEDX28_P 49
TR27_P 47
DEDX27_P 45
TR26_P 43
DEDX26_P 41
TR25_P 39
DEDX25_P 37
TR24_P 35
DEDX24_P 33
TR23_P 31
DEDX23_P 29
TR22_P 27
DEDX22_P 25
TR21_P 23
DEDX21_P 21
TR20_P 19
DEDX20_P 17
TR19_P 15
DEDX19_P 13
TR18_P 11
DEDX18_P 9
TR17_P 7
DEDX17_P 5
TR16_P 3
DEDX16_P 1
80 S4_N
78 S3_N
76 S2_N
74 S1_N
72
70 STROBE_N
68
66
64 TR31_N
62 DEDX31_N
60 TR30_N
58 DEDX30_N
56 TR29_N
54 DEDX29_N
52 TR28_N
50 DEDX28_N
48 TR27_N
46 DEDX27_N
44 TR26_N
42 DEDX26_N
40 TR25_N
38 DEDX25_N
36 TR24_N
34 DEDX24_N
32 TR23_N
30 DEDX23_N
28 TR22_N
26 DEDX22_N
24 TR21_N
22 DEDX21_N
20 TR20_N
18 DEDX20_N
16 TR19_N
14 DEDX19_N
12 TR18_N
10 DEDX18_N
8 TR17_N
6 DEDX17_N
4 TR16_N
2 DEDX16_N
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@DATETIME=8-15-1997_10:32
Brookhaven National Laboratory
Instrumentation Division
Upton, NY 11973
Approvals Date
Drawn
Checked
Issued
Drawing:
PHENIX Time Expansion Chamber
Preamp-Shaper Front End Electronics
SIZE B
DWG NO:
REV NO: 1
SCALE
TECPS Rev2 - 32 Channels
FEM Interface Connector and Serial Connector
Drawn By:
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Sheet: 46 of 46

#	QTY	REFDES	DEVICE	DECAL	VALUE
1	14	C1,C2,C3,C4, C5,C6,C7,C8, C9,C10,C11, C12,C13,C20	CAPTANT	3216	1U
2	7	C14,C17,C21, C23,C24,C25, C26	CAPTANT	6032	10U
3	5	C15,C16,C18, C19,C22	CAPTANT	7343	47U
4	114	C27,C28,C29, C30,C31,C32, C33,C34,C35, C36,C37,C38, C39,C40,C41, C42,C43,C44, C45,C46,C47, C48,C49,C50, C51,C52,C53, C54,C55,C56, C57,C58,C59, C60,C61,C62, C63,C64,C65, C66,C67,C68, C69,C70,C71, C72,C73,C74, C75,C76,C77, C78,C79,C80, C81,C82,C83, C84,C85,C86, C87,C88,C89, C90,C91,C92, C93,C94,C95, C96,C97,C98, C99,C100,C101, C102,C103, C104,C105, C106,C107, C108,C109, C110,C111, C112,C113, C114,C115, C116,C117, C118,C119, C120,C121, C122,C123, C124,C125, C126,C127, C128,C129, C130,C132, C133,C134, C135,C136, C137,C140, C141,C142,C143	CAPSMT	0603	0.1U
5	1	C131	CAPSMT	0603	220P
6	1	C138	CAPSMT	0805	390P
7	1	C139	CAPSMT	0805	47P
8	32	D1,D2,D3,D4, D5,D6,D7,D8, D9,D10,D11, D12,D13,D14, D15,D16,D17, D18,D19,D20, D21,D22,D23, D24,D25,D26,	BAV99ZX	SOT23D	

		D27,D28,D29, D30,D31,D32			
9	1	D33	DL4002	SOD-87	DL4002
10	1	E1	INP-HDR2	SIP-2P	
11	4	F1,F2,F3,F4	SMD050	MSMD075	500MA
12	1	J1	MOLEXW2B4	53398-0490	
13	1	J2	MOLEXW2B8	53398-0890	
14	3	JP1,JP2,JP3	JUMPER	SIP-2P	
15	2	L1,L2	BLA41B01	BLA41B01	000
16	4	L3,L4,L5,L6	BLM41A800	1805	000
17	1	M1	SST211	SOT143	
18	4	P1,P2,P3,P4	ZPACK24	223513-1	
19	2	P5,P6	IDC-HD	845-A080P-ALA55	
20	32	R1,R2,R3,R4, R5,R6,R7,R8, R9,R10,R11, R12,R13,R14, R15,R16,R17, R18,R19,R20, R21,R22,R23, R24,R25,R26, R27,R28,R29, R30,R31,R32	RESSMT	0603	24.9
21	64	R33,R35,R37, R39,R41,R43, R45,R47,R49, R51,R53,R55, R57,R59,R61, R63,R65,R67, R69,R71,R73, R75,R77,R79, R81,R83,R85, R87,R89,R91, R93,R95,R97, R99,R101,R103, R105,R107, R109,R111, R113,R115, R117,R119, R121,R123, R125,R127, R129,R131, R133,R135, R137,R139, R141,R143, R145,R147, R149,R151, R153,R155, R157,R159	RES_NW2	RES-EXB-V2	5.6K
22	64	R34,R36,R38, R40,R42,R44, R46,R48,R50, R52,R54,R56, R58,R60,R62, R64,R66,R68, R70,R72,R74, R76,R78,R80, R82,R84,R86, R88,R90,R92, R94,R96,R98, R100,R102, R104,R106, R108,R110, R112,R114, R116,R118, R120,R122, R124,R126, R128,R130, R132,R134, R136,R138,	RES_NW2	RES-EXB-V2	56

		R140,R142,			
		R144,R146,			
		R148,R150,			
		R152,R154,			
		R156,R158,R160			
23	64	R161,R162,	RESSMT	0603	51.1
		R163,R164,			
		R165,R166,			
		R167,R168,			
		R169,R170,			
		R171,R172,			
		R173,R174,			
		R175,R176,			
		R177,R178,			
		R179,R180,			
		R181,R182,			
		R183,R184,			
		R185,R186,			
		R187,R188,			
		R189,R190,			
		R191,R192,			
		R193,R194,			
		R195,R196,			
		R197,R198,			
		R199,R200,			
		R201,R202,			
		R203,R204,			
		R205,R206,			
		R207,R208,			
		R209,R210,			
		R211,R212,			
		R213,R214,			
		R215,R216,			
		R217,R218,			
		R219,R220,			
		R221,R222,			
		R223,R224			
24	2	R225,R226	RESSMT	0603	10K
25	1	R227	RESSMT	0603	51.1
26	1	R228	RESSMT	0603	47K
27	1	R229	RESSMT	0603	105K
28	1	R230	RESSMT	0603	102K
29	2	R231,R232	RESSMT	0603	121
30	4	U1,U2,U3,U4	IC31A-QFP	MQFP64-M108	
31	32	U5,U6,U7,U8,	AD8044AR	SO14M1	
		U9,U10,U11,			
		U12,U13,U14,			
		U15,U16,U17,			
		U18,U19,U20,			
		U21,U22,U23,			
		U24,U25,U26,			
		U27,U28,U29,			
		U30,U31,U32,			
		U33,U34,U35,			
		U36			
32	1	U37	DS26C32	SO16M1	
33	1	U38	SN74HC14	SO14M1	
34	1	U39	EPM7032QC	QFP44-5	
35	1	U40	DAC8562FS	SO20WB	
36	2	U41,U42	DS26C31	SO16M1	
37	1	U43	MIC29372BU	TO-263-5	
38	1	U44	LM337T	TO-220-S	
39	1	U45	MIC2937A	TO-263	
40	1	U46	LT1175CST-5	SOT-223	
41	1	U47	DS1624	SO8M1	

	478				

INSTRUMENTATION DIVISION
BROOKHAVEN NATIONAL LABORATORY
UPTON, NY 11973

JOB TITLE: PHENIX TEC Preamp/Shaper Front End board.

BNL-IO Control number: IO-865-1-2

JOB DESCRIPTION:

Design services for layout of multi-layer printed circuit board as per Brookhaven specifications.

ITEMS PROVIDED BY BNL:

1. Schematics.
2. PADS Perform / PADS Power PCB job file with the net-list read into the job.
3. Copy of the parts and decal library used in the Job file.
4. Available Datasheets for cross reference will be provided.
5. Earlier revision of an identical PCB designed at BNL will be provided for reference. [BNL/IO-849-1]

Engineer: Anand Kandasamy
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Phone: 516-344-5486
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Email: anand@bnl.gov

SPECIFACTION AND DESIGN RULES:

1. NO AUTO ROUTING TO BE PERFORMED.

2. Strict trace length minimization in the X direction.

3. Input traces which belong to the net class below should have minimum exposure.

   CHIPA_INPUTS, CHIPB_INPUTS, CHIPC_INPUTS and CHIPD_INPUTS

4. TOP and BOTTOM layers require maximum copper flood, connected to net GND.

5. Planes required:

Net VDD :	1	
Net VSS :	1	
Net VCC :	1	
Net VEE :	1	
Net GND :	3	[including TOP and BOTTOM GND Flood]
Signal :		As required by routing consideration.

6. Refer to BNL-JOB/IO849-1 for routing of net CALIB.

7. Net ~CLK and NET ~LD has to fan-out from the midpoint of chips A,B,C and D and has to be symmetric.

8. Trace capacitance of signals under the net class below has to be less than 10pF. Layer Stack up can be modified to achieve this.

   CMOS_DEDX and CMOS_TR

9. Maintain the placement strategy of the below components.

   D1-D32
   R1-R32

10. Every signal routing layers separated by power or ground plane.

11. Input power traces to the voltage regulators on segmented plane on any of the routing layers, instead of wide traces. [see BNL−JOB: IO−849−1, Layers 4, 5 and 8].

    These net are power carrying nets. +3*, 6V*

12. Tabs on U43 and U45 connected to GND plane/flood to act as heat sink. Tabs on U44 and U46 connected to their respective signals in the net−list and copper area connected to the tab made larger to dissipate heat.

13. 56 ohm Resistor packs on net class OUT_DEDX_P, OUT_DEDX_N, OUT_TR_P and OUT_TR_N has to be placed closer to the opamp where the signal originates.

    * Refer to BNL−JOB/IO849−1, for placement followed.

14. Test points for power VDD, VCC, VEE, VSS and GND to be placed at 100mil center.

15. Maintain the copper keep out area on all layers on the edge of the board, as in BNL−JOB : IO−849−1.

16. Layer numbering window [see BNL−JOB: IO−849−1].

17. Solder mask and Silk screen−Legend required.

18. PADSTACK has to be verified by the Layout designer for every part, even though parts were supplied by BNL

19. Board Thickness : 0.093"

20. Total Number of Boards required: 20

21. Treat all trace width to be FINISHED trace width.

Signals that are treated as differential pairs and net class assignments are given below.

DIFFERENTIAL PAIRS

[NET_PAIR]	DEDX0_N	DEDX0_P
[NET_PAIR]	DEDX1_N	DEDX1_P
[NET_PAIR]	DEDX2_N	DEDX2_P
[NET_PAIR]	DEDX3_N	DEDX3_P
[NET_PAIR]	DEDX4_N	DEDX4_P
[NET_PAIR]	DEDX5_N	DEDX5_P
[NET_PAIR]	DEDX6_N	DEDX6_P
[NET_PAIR]	DEDX7_N	DEDX7_P
[NET_PAIR]	DEDX8_N	DEDX8_P
[NET_PAIR]	DEDX9_N	DEDX9_P
[NET_PAIR]	DEDX10_N	DEDX10_P
[NET_PAIR]	DEDX11_N	DEDX11_P
[NET_PAIR]	DEDX12_N	DEDX12_P
[NET_PAIR]	DEDX13_N	DEDX13_P
[NET_PAIR]	DEDX14_N	DEDX14_P
[NET_PAIR]	DEDX15_N	DEDX15_P
[NET_PAIR]	DEDX16_N	DEDX16_P
[NET_PAIR]	DEDX17_N	DEDX17_P
[NET_PAIR]	DEDX18_N	DEDX18_P
[NET_PAIR]	DEDX19_N	DEDX19_P
[NET_PAIR]	DEDX20_N	DEDX20_P
[NET_PAIR]	DEDX21_N	DEDX21_P
[NET_PAIR]	DEDX22_N	DEDX22_P
[NET_PAIR]	DEDX23_N	DEDX23_P
[NET_PAIR]	DEDX24_N	DEDX24_P

```
[NET_PAIR]      DEDX25_N        DEDX25_P
[NET_PAIR]      DEDX26_N        DEDX26_P
[NET_PAIR]      DEDX27_N        DEDX27_P
[NET_PAIR]      DEDX28_N        DEDX28_P
[NET_PAIR]      DEDX29_N        DEDX29_P
[NET_PAIR]      DEDX30_N        DEDX30_P
[NET_PAIR]      DEDX31_N        DEDX31_P
[NET_PAIR]      TR0_N           TR0_P
[NET_PAIR]      TR1_N           TR1_P
[NET_PAIR]      TR2_N           TR2_P
[NET_PAIR]      TR3_N           TR3_P
[NET_PAIR]      TR4_N           TR4_P
[NET_PAIR]      TR5_N           TR5_P
[NET_PAIR]      TR6_N           TR6_P
[NET_PAIR]      TR7_N           TR7_P
[NET_PAIR]      TR8_N           TR8_P
[NET_PAIR]      TR9_N           TR9_P
[NET_PAIR]      TR10_N          TR10_P
[NET_PAIR]      TR11_N          TR11_P
[NET_PAIR]      TR12_N          TR12_P
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[NET_PAIR]      TR15_N          TR15_P
[NET_PAIR]      TR16_N          TR16_P
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[NET_PAIR]      TR28_N          TR28_P
[NET_PAIR]      TR29_N          TR29_P
[NET_PAIR]      TR30_N          TR30_P
[NET_PAIR]      TR31_N          TR31_P
[NET_PAIR]      INA+            INA−
[NET_PAIR]      INB+            INB−
[NET_PAIR]      INC+            INC−
[NET_PAIR]      STR+            STR−
[NET_PAIR]      S1_N            S1_P
[NET_PAIR]      S2_N            S2_P
[NET_PAIR]      S3_N            S3_P
[NET_PAIR]      S4_N            S4_P
[NET_PAIR]      RDBK_N          RDBK_P
[NET_PAIR]      CLK_N           CLK_P
[NET_PAIR]      DATA_N          DATA_P
[NET_PAIR]      LD_N            LD_P
[NET_PAIR]      STROBE_N        STROBE_P


NET_CLASS CHIPA_INPUTS

        ANODE0 ANODE1 ANODE2 ANODE3 ANODE4 ANODE5 ANODE6 ANODE7
        IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7

NET_CLASS CHIPB_INPUTS

        ANODE8 ANODE9 ANODE10 ANODE11 ANODE12 ANODE13 ANODE14 ANODE15
        IN8 IN9 IN10 IN11 IN12 IN13 IN14 IN15

NET_CLASS CHIPC_INPUTS

        ANODE16 ANODE17 ANODE18 ANODE19 ANODE20 ANODE21 ANODE22 ANODE23
        IN16 IN17 IN18 IN19 IN20 IN21 IN22 IN23

NET_CLASS CHIPD_INPUTS
```

```
        ANODE24 ANODE25 ANODE26 ANODE27 ANODE28 ANODE29 ANODE30 ANODE31
        IN24 IN25 IN26 IN27 IN28 IN29 IN30 IN31

NET_CLASS SERIAL

        CLK_N CLK_P DATA DATA_N DATA_P DIN DOUTA DOUTB DOUTC DOUTD
        INA+ INA- INB+ INB- INC+ INC- LD_N LD_P MODE OUTA OUTAB
        OUTB OUTBB OUTC OUTCB RDBK_N RDBK_P STR+ STR- STROBE_N STROBE_P
        ~CLK ~CLOCK ~LD ~LOAD

NET_CLASS CALIBRATION

        CALIB DACOUT EXT_CAL INT_CAL STROBE VX10

NET_CLASS DAC

        BIT0 BIT1 BIT2 BIT3 BIT4 BIT5 BIT6 BIT7 BIT8 BIT9 BIT10 BIT11

NET_CLASS OPAMP_PWR+

        V+U5 V+U6 V+U7 V+U8 V+U9 V+U10 V+U11 V+U12
        V+U13 V+U14 V+U15 V+U16 V+U17 V+U18 V+U19 V+U20
        V+U21 V+U22 V+U23 V+U24 V+U25 V+U26 V+U27 V+U28
        V+U29 V+U30 V+U31 V+U32 V+U33 V+U34 V+U35 V+U36

NET_CLASS OPAMP_PWR-

        V-U5 V-U6 V-U7 V-U8 V-U9 V-U10 V-U11 V-U12
        V-U13 V-U14 V-U15 V-U16 V-U17 V-U18 V-U19 V-U20
        V-U21 V-U22 V-U23 V-U24 V-U25 V-U26 V-U27 V-U28
        V-U29 V-U30 V-U31 V-U32 V-U33 V-U34 V-U35 V-U36

NET_CLASS BIAS

        IBIAS_A IBIAS_B IBIAS_C IBIAS_D
        OBIAS_A OBIAS_B OBIAS_C OBIAS_D
        RBIAS_A RBIAS_B RBIAS_C RBIAS_D
        VB1_A VB1_B VB1_C VB1_D
        VB2_A VB2_B VB2_C VB2_D

NET_CLASS ADDRESS

        S1 S1_N S1_P S2 S2_N S2_P S3 S3_N S3_P S4 S4_N S4_P

NET_CLASS PWR_INPUTS

        3V+ 3V+F 3V+L 6V+ 6V+F 6V+L 6V- 6V-FA 6V-FB 6V-LA 6V-LB

NET_CLASS PWR_VDD

        VDD VDD_ADJ

NET_CLASS PWR_VSS

        VSS VSS_ADJ

NET_CLASS PWR_VCC

        VCC

NET_CLASS PWR_VEE

        VEE

NET_CLASS DS1624

        GND_EXT SCL SDA VCC_EXT

NET_CLASS OUT_DEDX_P
```

```
        DEDX0_P DEDX1_P DEDX2_P DEDX3_P DEDX4_P DEDX5_P DEDX6_P DEDX7_P
        DEDX8_P DEDX9_P DEDX10_P DEDX11_P DEDX12_P DEDX13_P DEDX14_P
        DEDX15_P DEDX16_P DEDX17_P DEDX18_P DEDX19_P DEDX20_P DEDX21_P
        DEDX22_P DEDX23_P DEDX24_P DEDX25_P DEDX26_P DEDX27_P DEDX28_P
        DEDX29_P DEDX30_P DEDX31_P

NET_CLASS OUT_DEDX_N

        DEDX0_N DEDX1_N DEDX2_N DEDX3_N DEDX4_N DEDX5_N DEDX6_N DEDX7_N
        DEDX8_N DEDX9_N DEDX10_N DEDX11_N DEDX12_N DEDX13_N DEDX14_N
        DEDX15_N DEDX16_N DEDX17_N DEDX18_N DEDX19_N DEDX20_N DEDX21_N
        DEDX22_N DEDX23_N DEDX24_N DEDX25_N DEDX26_N DEDX27_N DEDX28_N
        DEDX29_N DEDX30_N DEDX31_N

NET_CLASS OUT_TR_N

        TR0_N TR1_N TR2_N TR3_N TR4_N TR5_N TR6_N TR7_N TR8_N TR9_N
        TR10_N TR11_N TR12_N TR13_N TR14_N TR15_N TR16_N TR17_N TR18_N
        TR19_N TR20_N TR21_N TR22_N TR23_N TR24_N TR25_N TR26_N TR27_N
        TR28_N TR29_N TR30_N TR31_N

NET_CLASS OUT_TR_P

        TR0_P TR1_P TR2_P TR3_P TR4_P TR5_P TR6_P TR7_P TR8_P TR9_P
        TR10_P TR11_P TR12_P TR13_P TR14_P TR15_P TR16_P TR17_P TR18_P
        TR19_P TR20_P TR21_P TR22_P TR23_P TR24_P TR25_P TR26_P TR27_P
        TR28_P TR29_P TR30_P TR31_P

NET_CLASS CMOS_TR

        TR0 TR1 TR2 TR3 TR4 TR5 TR6 TR7 TR8 TR9 TR10 TR11 TR12 TR13 TR14
        TR15 TR16 TR17 TR18 TR19 TR20 TR21 TR22 TR23 TR24 TR25 TR26 TR27
        TR28 TR29 TR30 TR31

NET_CLASS CMOS_DEDX

        DEDX0 DEDX1 DEDX2 DEDX3 DEDX4 DEDX5 DEDX6 DEDX7 DEDX8 DEDX9 DEDX10
        DEDX11 DEDX12 DEDX13 DEDX14 DEDX15 DEDX16 DEDX17 DEDX18 DEDX19
        DEDX20 DEDX21 DEDX22 DEDX23 DEDX24 DEDX25 DEDX26 DEDX27 DEDX28
        DEDX29 DEDX30 DEDX31

NET_CLASS OPAMP_DEDX_POS

        D0P D1P D2P D3P D4P D5P D6P D7P D8P D9P D10P D11P D12P D13P D14P
        D15P D16P D17P D18P D19P D20P D21P D22P D23P D24P D25P D26P D27P
        D28P D29N D30P D31P

NET_CLASS OPAMP_DEDX_NEG

        D0N D1N D2N D3N D4N D5N D6N D7N D8N D9N D10N D11N D12N D13N D14N
        D15N D16N D17N D18N D19N D20N D21N D22N D23N D24N D25N D26N D27N
        D28N D29P D30N D31N

NET_CLASS OPAMP_DEDX_INN

        D0INN D1INN D2INN D3INN D4INN D5INN D6INN D7INN D8INN D9INN D10INN
        D11INN D12INN D13INN D14INN D15INN D16INN D17INN D18INN D19INN
        D20INN D21INN D22INN D23INN D24INN D25INN D26INN D27INN D28INN
        D29INN D30INN D31INN

NET_CLASS OPAMP_TR_INN

        T0INN T1INN T2INN T3INN T4INN T5INN T6INN T7INN T8INN T9INN T10INN
        T11INN T12INN T13INN T14INN T15INN T16INN T17INN T18INN T19INN
        T20INN T21INN T22INN T23INN T24INN T25INN T26INN T27INN T28INN
        T29INN T30INN T31INN

NET_CLASS OPAMP_TR_NEG
```

```
        T0N T1N T2N T3N T4N T5N T6N T7N T8N T9N T10N T11N T12N T13N T14N
        T15N T16N T17N T18N T19N T20N T21N T22N T23N T24N T25N T26N T27N
        T28N T29N T30N T31N

NET_CLASS OPAMP_TR_POS

        T0P T1P T2P T3P T4P T5P T6P T7P T8P T9P T10P T11P T12P T13P T14P
        T15P T16P T17P T18P T19P T20P T21P T22P T23P T24P T25P T26P T27P
        T28P T29P T30P T31P

NET_CLASS PWR_GND

        GND
```

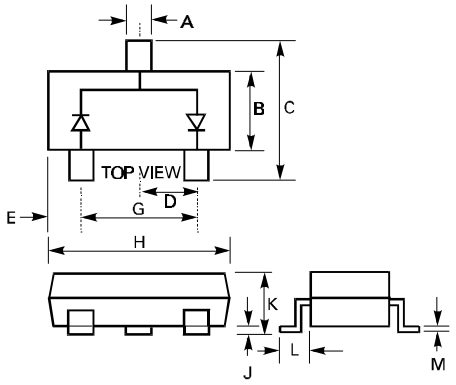
BAV99

SURFACE MOUNT SWITCHING DIODE

Features

- High Conductance
- Ultra Fast Switching Time
- Dual Diode in Series (Doubler) Connection

SOT-23



	Min	Max
A	0.37	0.50
B	1.19	1.409
C	2.10	2.50
D	0.89	1.05
E	0.45	0.61
G	1.78	2.05
H	2.79	3.05
J	0.013	0.150
K	0.89	1.10
L	0.45	0.61
M	0.076	0.130
All Dimensions in mm		

Mechanical Data

- Case: SOT-23 Plastic
- Terminals: Solderable per MIL-STD-202, Method 208
- Mounting Position: Any
- Weight: 0.01 grams (approx.)

Alternate Marking Codes:
A7, JE, RA7, RBA

Maximum Ratings

Single Diode

Characteristic	Symbol	Value	Unit
Power Dissipation @ T_A = 25°C for Total Package (Mounted)	P_d	300	mW
Reverse Voltage, Peak Reverse Voltage	V_R, V_{RM}	70	V
Peak Forward Current	I_{FM}	300	mA
Average Rectified Current	I_{AV}	100	mA
Peak Forward Surge Current Pulse Width = 1μSec Pulse Width = 1 Second	I_{FSM}	 2.0 0.5	 A A
Storage & Operating Temperature	T_j, T_{STG}	-55 to +150	°C

Electrical Characteristics

Single Diode @ T_A = 25°C Unless otherwise specified

Characteristic	Test Conditions	Symbol	Min	Max	Unit
Breakdown Voltage	I_R = 100μA	$V_{(BR)}$	70		V
Reverse Current	V_R = 70V V_R = 25V, T_A = 150°C V_R = 70V, T_A = 150°C	I_R	—	2.5 50 100	μA
Forward Voltage	I_F = 1.0mA I_F = 10mA I_F = 50mA I_F = 150mA	V_F	—	715 0.855 1.1 1.25	mV V V V
Reverse Recovery Time	I_F = I_R = 10mA I_{RR} = 1.0mA R_L = 100Ω	T_{rr}	—	6.0	nSec
Diode Capacitance	V_F = V_R = 0 f = 1MHz	C_T	—	4.0	pF

To order/reorder this document please request Data Sheet BAV99 Rev. B 5/15/96 or Data Sheet BAV99 (Current Revision).

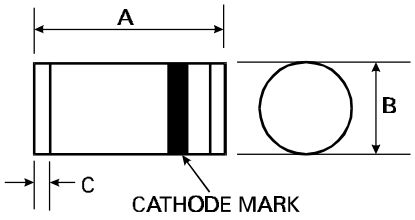
DL4001 - DL4007

1.0 AMPERE GLASS PASSIVATED SURFACE MOUNT RECTIFIER

Features

- Glass passivated junction
- Plastic material has Underwriters Lab flammability Classfication 94V-0
- High current capability
- Low forward voltage drop
- High reliability and low leakage
- For surface mounted application

MELF



	Min	Max
A	4.8	5.2
B	2.4	2.5
C	0.55∅ Nominal	
All dimensions in mm		

Mechanical Data

- TERMINALS: Solderable per MIL-STD-202, Method 208
- CASE: MELF, Molded Plastic
- MOUNTING POSITION: Any
- POLARITY: Cathode band

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60Hz, resistive or inductive load.

Characteristic	Symbol	DL4001	DL4002	DL4003	DL4004	DL4005	DL4006	DL4007	Unit
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	V_{RSM}	35	70	140	280	420	560	700	V
Maximum DC Blocking Voltage	V_{DC}	50	100	200	400	600	800	1000	V
Maximum Average Forward Rectified Current @ Terminal Temp (T_T) = 75°C	$I_{(AV)}$	1.0							A
Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	30							A
Maximum Forward Voltage at 1.0A	V_F	1.1							V
Maximum dc Reverse Current at T_A = 25°C Rated dc Blocking Voltage T_A = 100°C	I_R	5.0 50							μA μA
Typical Thermal Resistance (Note 1)	$R_{\theta JA}$	50							°C/W
Typical Junction Capacitance (Note 2)	C_J	15							pF
Storage and Operating Temperature Range	T_J, T_{STG}	-65 to +175							°C

NOTE: 1. Thermal resistance from junction to ambient.
2. Measured at 1MHz and applied reverse voltage of 4.0 volts.

To order/reorder this document please request Data Sheet DL4001 Rev. B 5/8/96 or Data Sheet DL4001 (Current Revision).

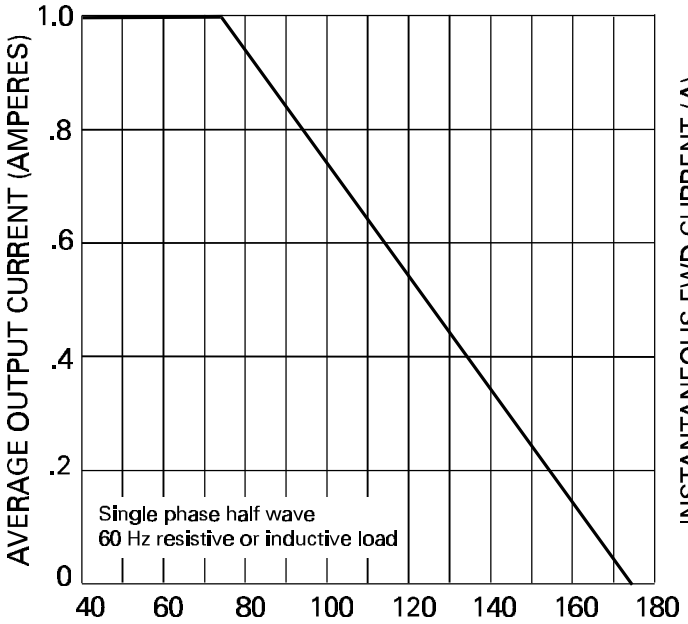


Fig. 1 Forward Current Derating Curve

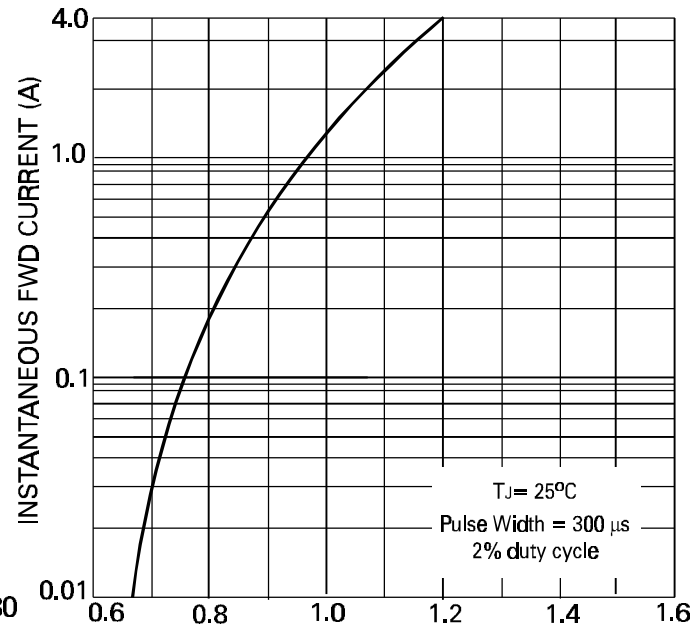


Fig. 2 Typical Forward Characteristics

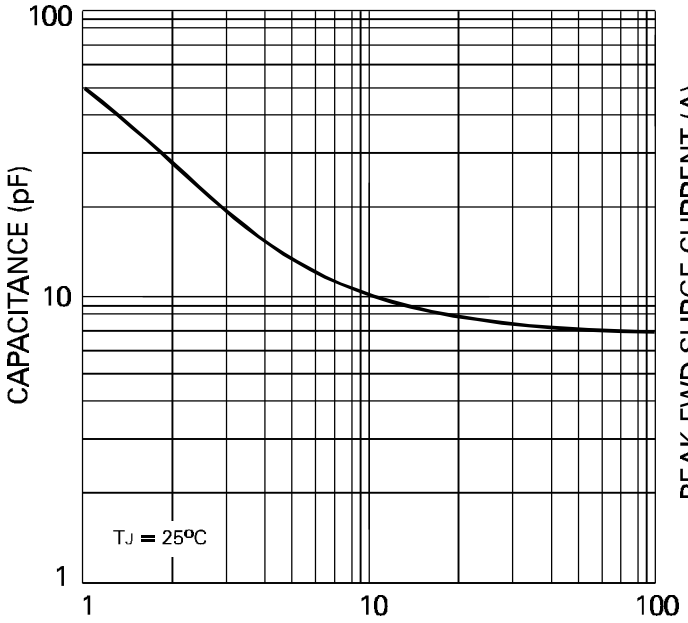


Fig. 3 Typical Junction Capacitance

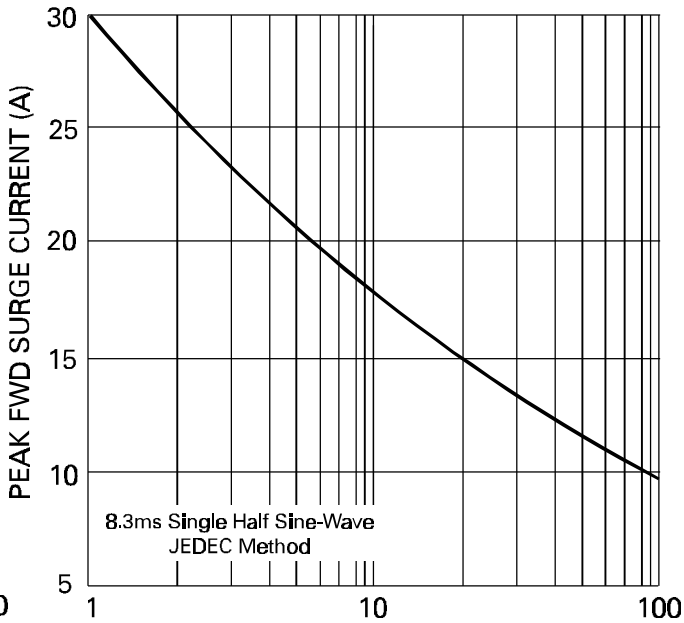


Fig. 4 Max Non-Repetitive Peak Fwd Surge Current

TEMIC

Siliconix

SD211DE/SST211 Series

N-Channel Lateral DMOS FETs

SD211DE SST211
SD213DE SST213
SD215DE SST215

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ V_{GS} = 10 V	0.5	2
SD213DE	10	1.5	45 @ V_{GS} = 10 V	0.5	2
SD215DE	20	1.5	45 @ V_{GS} = 10 V	0.5	2
SST211	30	1.5	50 @ V_{GS} = 10 V	0.5	2
SST213	10	1.5	50 @ V_{GS} = 10 V	0.5	2
SST215	20	1.5	50 @ V_{GS} = 10 V	0.5	2

For applications information see AN301, page 33.

Features

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

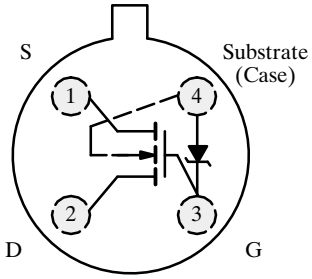
- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD211 may be used for ±5-V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An integrated Zener diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series and non-Zener protection—SD210DE/214DE.

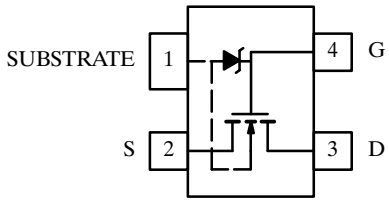
TO-206AF
(TO-72)



Top View

SD211DE, SD213DE, SD215DE

TO-253
(SOT-143)



Top View

SST211 (D1)*, SST213 (D3)*, SST215 (D5)*

*Marking Code for TO-253

SD211DE/SST211 Series

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage (SD211DE/SST211) . . −30/25 V
(SD213DE/SST213) . . −15/25 V
(SD215DE/SST215) . . −25/30 V

Gate-Substrate Voltage[a] (SD211DE/SST211) . . . . . −0.3/25 V
(SD213DE/SST213) . . . . . −0.3/25 V
(SD215DE/SST215) . . . . . −0.3/30 V

Drain-Source Voltage (SD211DE/SST211) . . . . . 30 V
(SD213DE/SST213) . . . . . 10 V
(SD215DE/SST215) . . . . . 20 V

Source-Drain Voltage (SD211DE/SST211) . . . . . 10 V
(SD213DE/SST213) . . . . . 10 V
(SD215DE/SST215) . . . . . 20 V

Drain-Substrate Voltage (SD211DE/SST211) . . . . . 30 V
(SD213DE/SST213) . . . . . 15 V
(SD215DE/SST215) . . . . . 25 V

Source-Substrate Voltage (SD211DE/SST211) . . . . . 15 V
(SD213DE/SST213) . . . . . 15 V
(SD215DE/SST215) . . . . . 25 V

Drain Current . . . . . 50 mA

Lead Temperature ($^1/_{16}$" from case for 10 seconds) . . . . . 300°C

Storage Temperature . . . . . −65 to 150°C

Operating Junction Temperature . . . . . −55 to 125°C

Power Dissipation[a] . . . . . 300 mW

Notes:
a. Derate 3 mW/°C above 25°C

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211 Series Min	211 Series Max	213 Series Min	213 Series Max	215 Series Min	215 Series Max	Unit
Static											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10$ µA		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source Open		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain Open		35	15		15		25		
Drain-Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$V		0.01		100		100		100	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 1$ µA, $V_{SB} = 0$ V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0$ V, $I_D = 1$ mA	$V_{GS} = 5$ V (SD Series)	58		70		70		70	Ω
			$V_{GS} = 5$ V (SST Series)	60		75		75		75	
			$V_{GS} = 10$ V (SD Series)	38		45		45		45	
			$V_{GS} = 10$ V (SST Series)	40		50		50		50	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							

Specifications[a]

Parameter	Symbol[b]	Test Conditions[b]		Typ[c]	Limits 211 Series Min	211 Series Max	213 Series Min	213 Series Max	215 Series Min	215 Series Max	Unit
Dynamic											
Forward Transconductance	g_{fs}	V_{DS} = 10 V V_{SB} = 0 V I_D = 20 mA, f = 1 kHz	SD Series	11	10		10		10		mS
			SST Series	10.5	9		9		9		
	g_{os}		A11	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	V_{DS} = 10 V f = 1 MHz V_{GS} = V_{BS} = −15 V	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
			SST Series	4.2							
Reverse Transfer Capacitance	C_{rss}		SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{d(on)}$	SD Series Only V_{SB} = 0 V, V_{IN} 0 to 5 V, R_G = 25 Ω V_{DD} = 5 V, R_L = 680 Ω		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{d(off)}$			2							
	t_f			6							

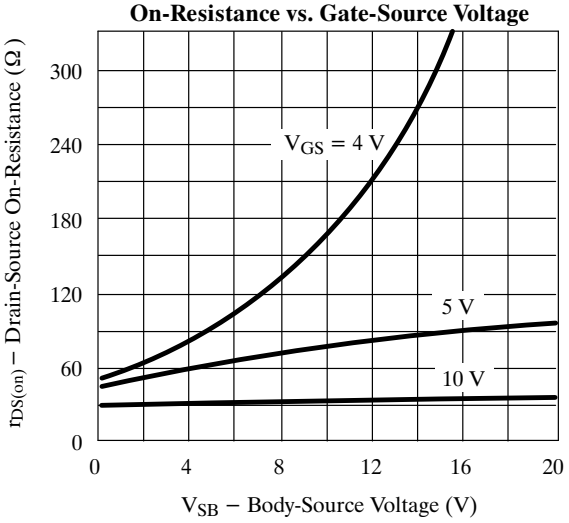
Notes:
a. T_A = 25°C unless otherwise noted.
b. B is the body (substrate), and (BR) is breakdown.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DMCBA

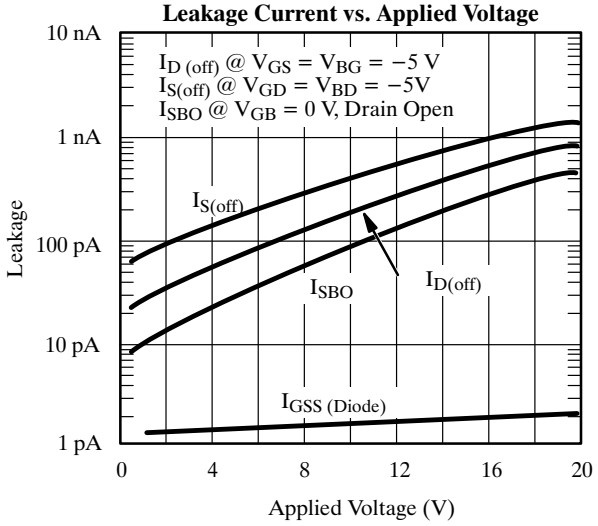
SD211DE/SST211 Series

Typical Characteristics

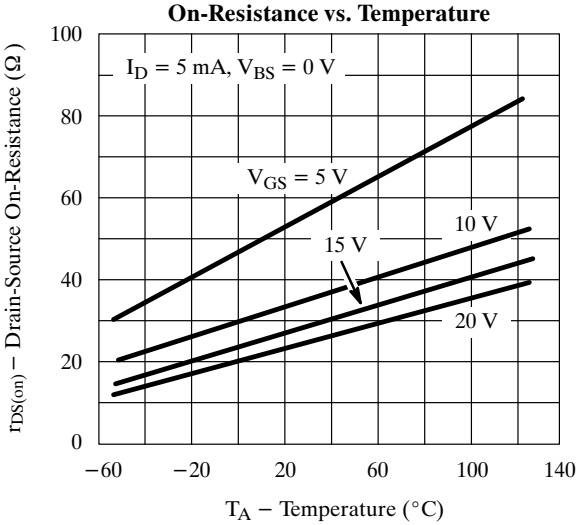
On-Resistance vs. Gate-Source Voltage



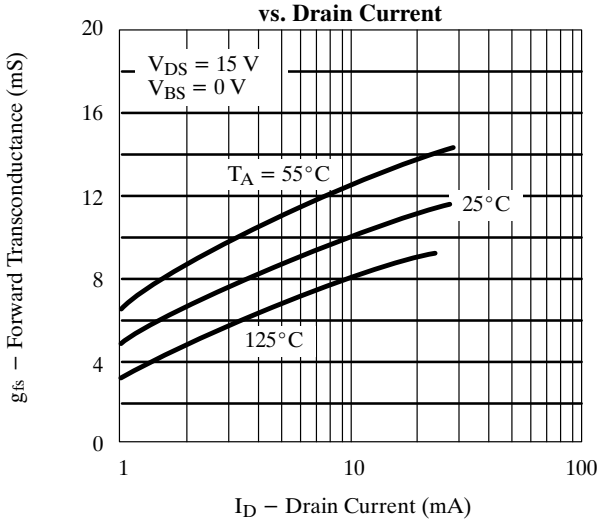
Leakage Current vs. Applied Voltage



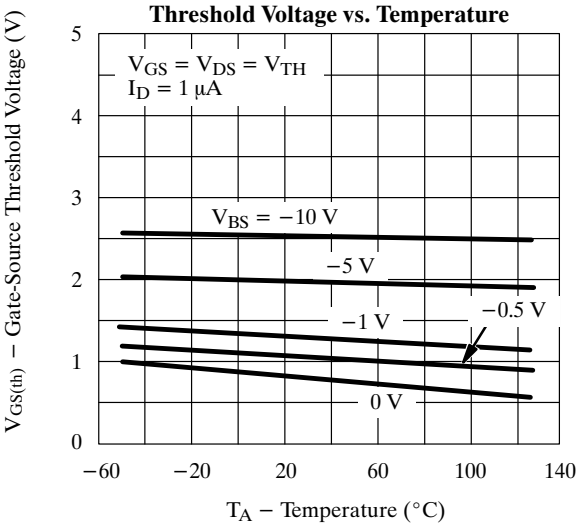
On-Resistance vs. Temperature



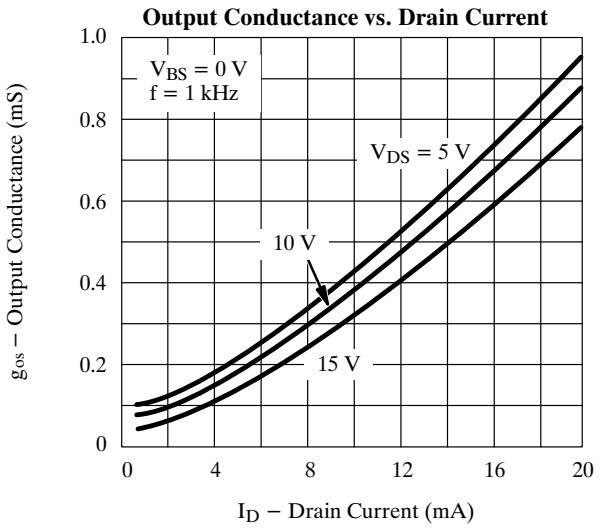
Common-Source Forward Transconductance vs. Drain Current



Threshold Voltage vs. Temperature

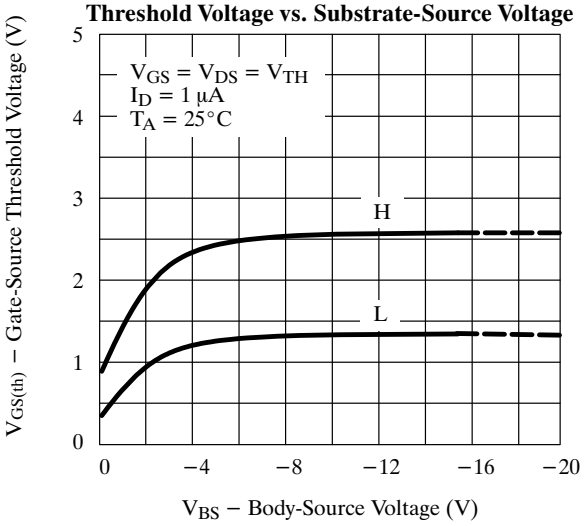


Output Conductance vs. Drain Current

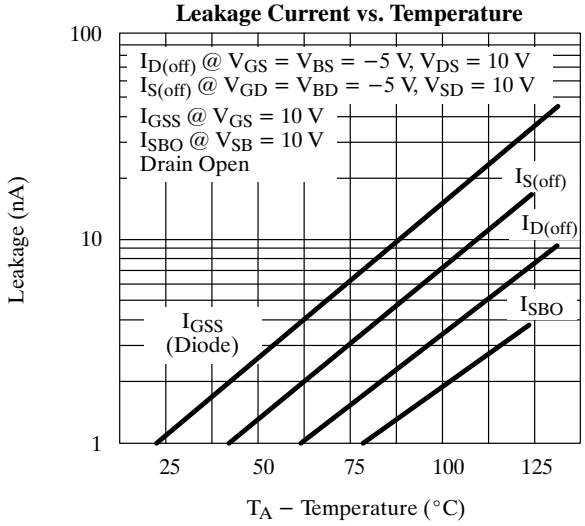


Typical Characteristics (Cont'd)

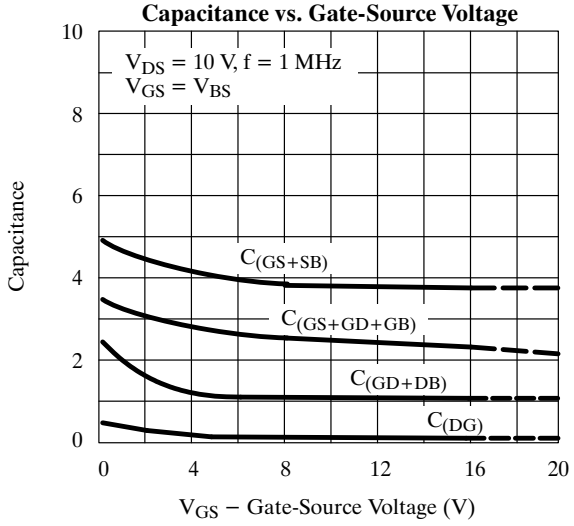
Threshold Voltage vs. Substrate-Source Voltage



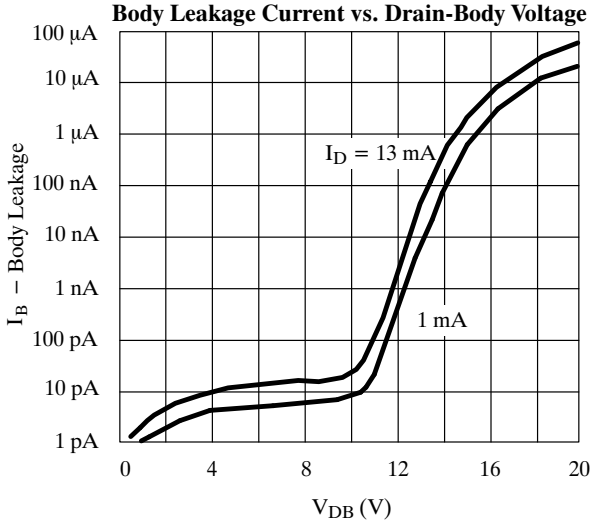
Leakage Current vs. Temperature



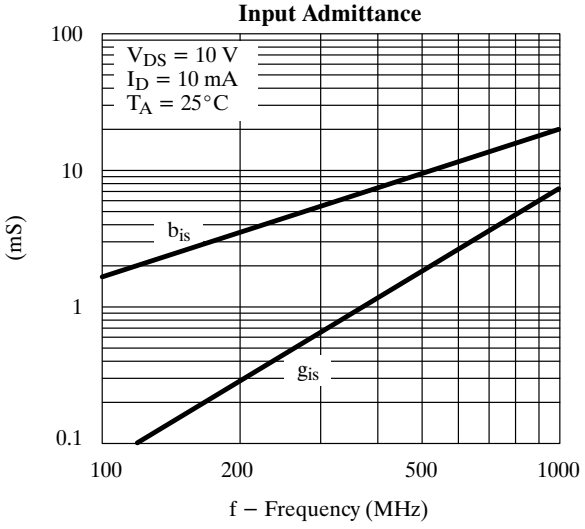
Capacitance vs. Gate-Source Voltage



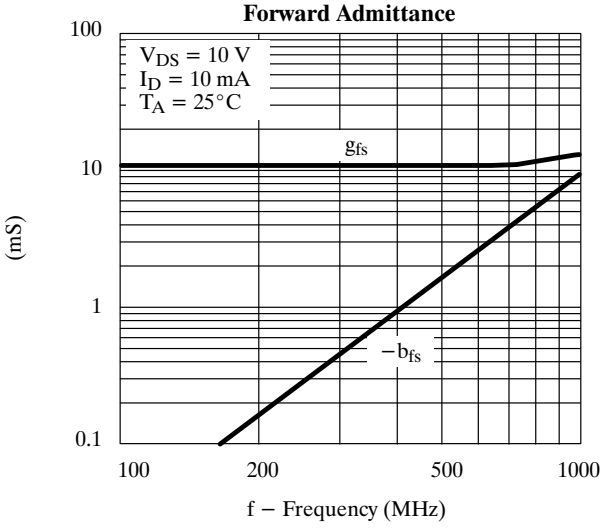
Body Leakage Current vs. Drain-Body Voltage



Input Admittance

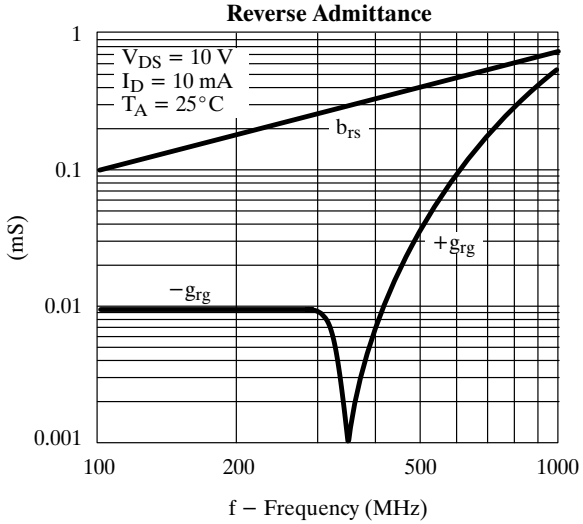


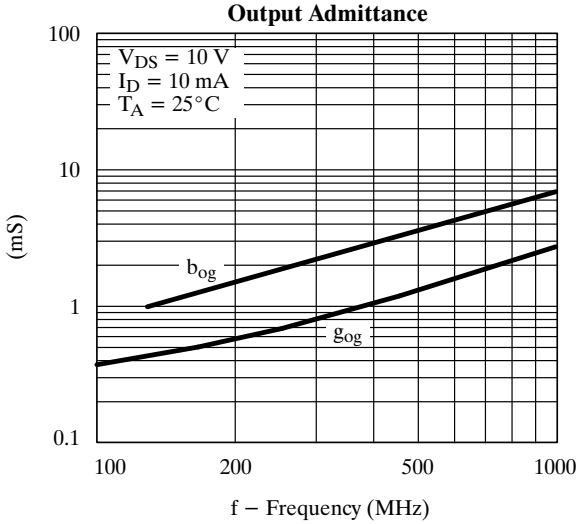
Forward Admittance

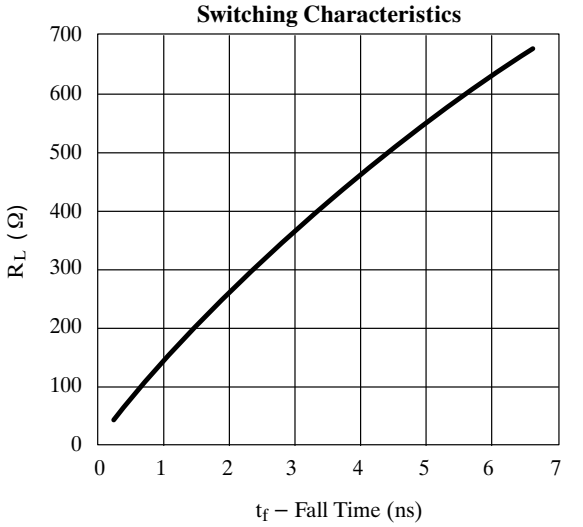


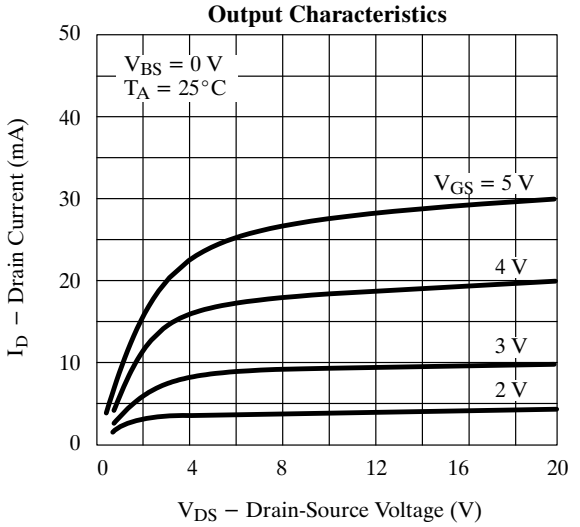
SD211DE/SST211 Series

Typical Characteristics

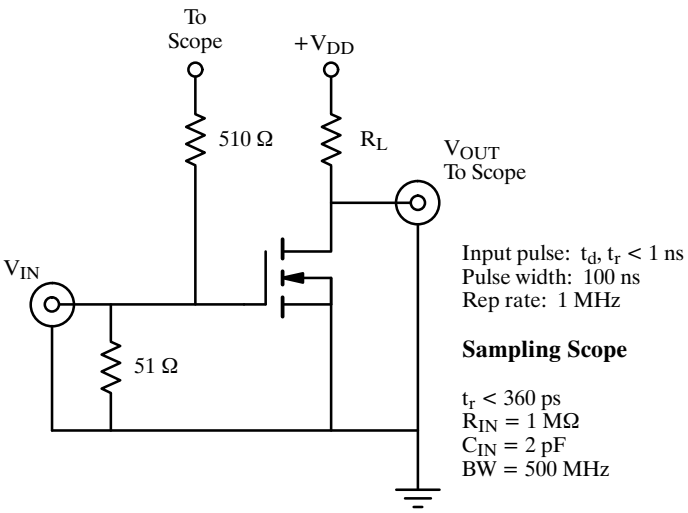


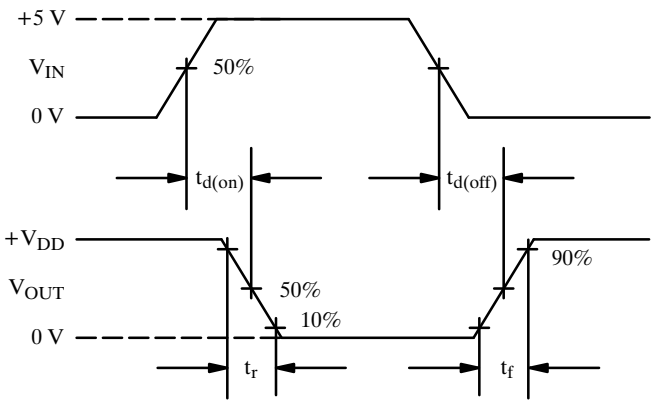






Switching Time Test Circuit

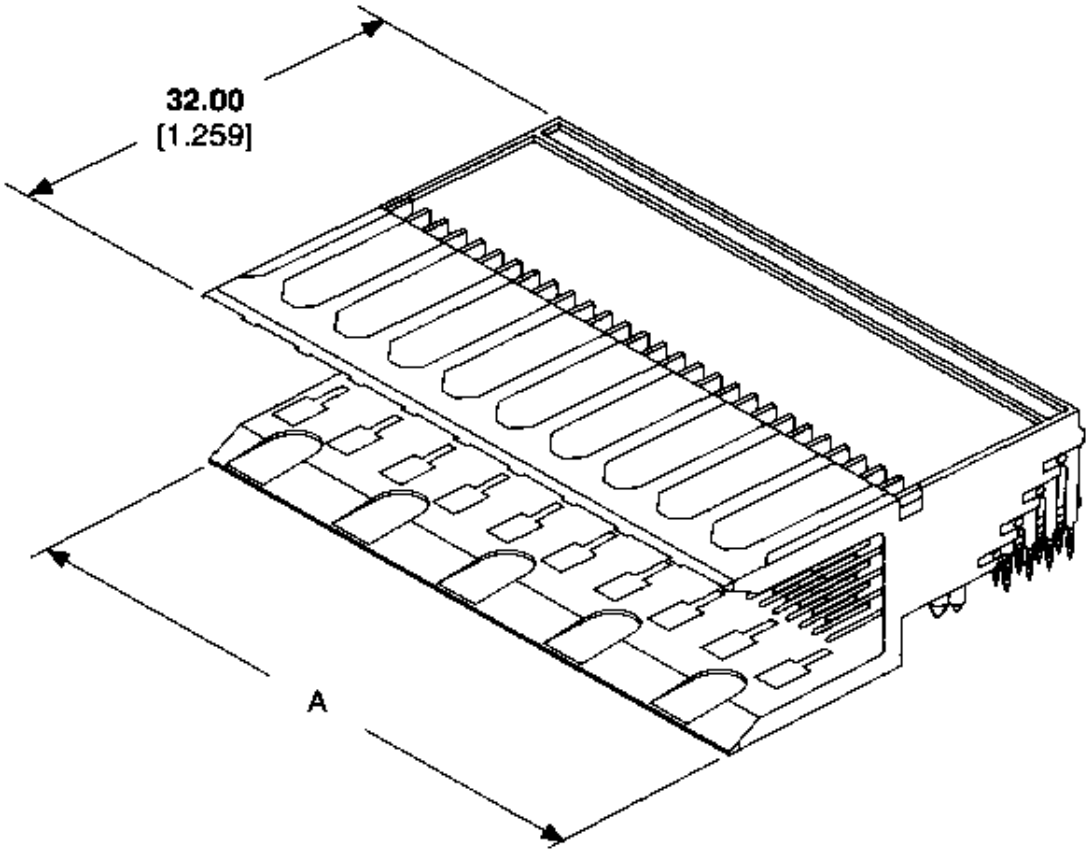




223513-1 -- *1 of 1 products*

General INFO
Sales INFO
Assembly SUBCONTRACTORS
Documentation

High Speed Connectors
Z-PACK 2mm FB (Futurebus+) Connectors

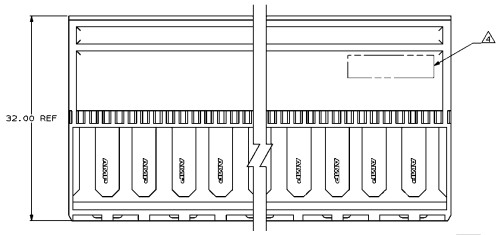


Line art represents typical product only.

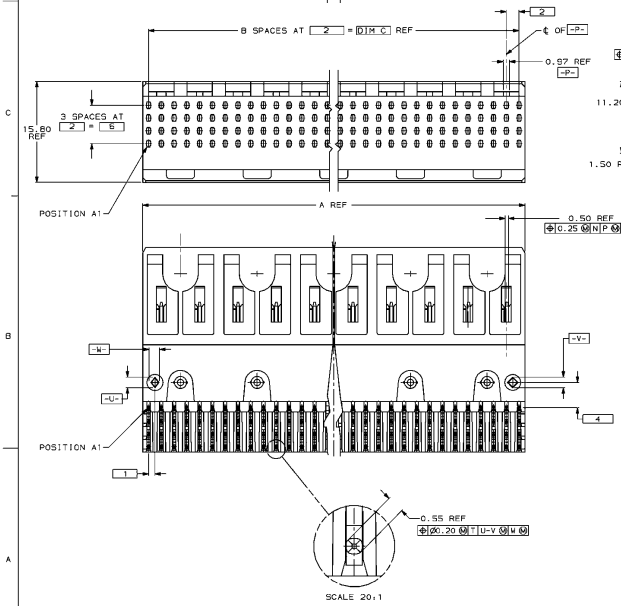
- Line Art
- Rec. PC Bd Hole Layout

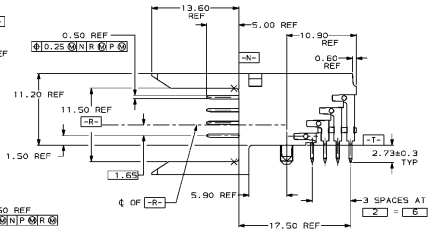
Searchable Features:	
# of Positions	24
Mating Type	Receptacle Assembly
Connector Type	Free-Board (Receptacle)
Module Type	Signal
PCB Mount Angle	Right Angle
Post Length	.115 [2.92] in. [mm]
Post Type	Solder Post
Shunted	No
Other Properties:	
Dim. A	.468 [11.88] in. [mm]
Dim. B	.394 [10.00] in. [mm]
Centerline Spacing	.079 [2.00] x .079 [2.00] in. [mm]
Contact Material	Phosphor Bronze
Contact Mating Area Plating	Gold Flash over Palladium-Nickel
Solder Tail Plating	Tin-Lead
Housing Material	Liquid Crystal Polymer (LCP)

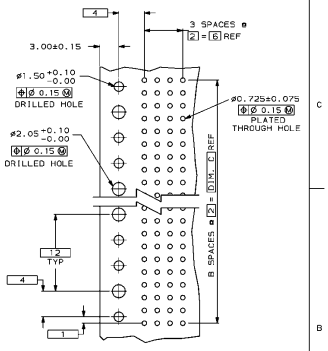
REVISIONS					
LTR	DESCRIPTION	DATE	DWN	APVD
D	REVISED PER ECN 0503-0039-97	28JAN97	JDL	SAS



1. HOUSING MATERIAL: LIQUID CRYSTAL POLYMER
   COLOR: NATURAL.
2. CONTACT MATERIAL: PHOSPHOR BRONZE PER UNS ALLOY NO. C51100, TEMPER: H04.
3. CONTACT FINISH:
   UNDERPLATE (ENTIRE CONTACT)-
   0.0013 MIN NICKEL
   ON MATING SURFACES-
   FLASH GOLD PER AMP INCORPORATED SPECIFICATION, OVER
   0.0008 MIN PALLADIUM-NICKEL PER AMP INCORPORATED SPECIFICATION, OVER
   UNDERPLATE.
   ON LEADS-
   0.0039 MIN TIN-LEAD, OVER
   UNDERPLATE.
   SURFACE CONDITIONER PER AMP SPECIFICATION 112-1002(ENTIRE CONTACT AFTER PLATING).
4. PART MARKING LOCATED APPROXIMATELY AS SHOWN.
5. NOT RELEASED FOR PRODUCTION.
6. PART TO BE MARKED WITH DATE CODE ONLY.







RECOMMENDED CIRCUIT PATTERN
PER IPC-D300 TYPE II, CLASS C
(COMPONENT SIDE)

C	B	A	NO. OF POSN	PART NUMBER
34	17	35.88	72	223513-7
58	29	59.88	120	223513-6
70	35	71.88	144	223513-5
94	47	55.88	192	223513-4
46	23	47.88	96	223513-3
22	11	23.88	48	223513-2
10	5	11.88	24	223513-1

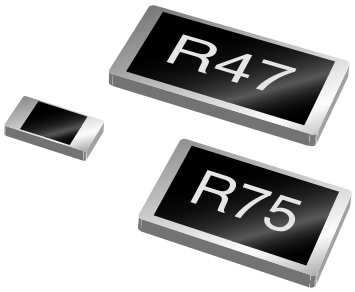
DR	R. WINCHESTER	28JAN97	AMP Incorporated Harrisburg, PA 17105-3608
DES	D. BACCHILE	28JAN97	
CHK	D. BACCHILE	28JAN97	
APVD			ASSEMBLY, PIN, SIGNAL, RIGHT ANGLE, 4 ROW, Z-PACK 2mm FB
SIZE	CAGE CODE	DRAWING NO	
A1	00779	C-223513	
SCALE 4:1	SHEET 1 OF 1	REV D	

CUSTOMER DRAWING

Thick Film Chip Resistors

Type ERJ

ERJ, 2G, 3G, 6G, 8G, 14, 12, 1W



Features

- **Small size and lightweight**
  For PCB size reduction and lightweight products
- **High reliability**
  Metal glaze thick film resistive element and three layers of electrodes result in high reliability
- **Matching with placement machine**
  Bulk, taping, and bulk case packagings for automatic placement machine
- **Solderability**
  Suitable for both reflow soldering and flow soldering
- **High power**
  One rank up approval of power rating is available for 3G, 6G, 8G type
- Approved under the ISO-9001 system

Conforming to: IEC115-8, JIS C225

Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11	12
E	R	J	8	G	E	J	J	1	0	2	
Product Code			Power Rating			Marking	Resistance Tolerance	Nominal Resistance Value			Packaging

Product Code

Thick Film Resistor Networks

Power Rating

2GE	1/16W
3GS	1/16W
6GE	1/10W
8GE	1/8W
14	1/4W
12	1/2W
1W	1 W

Marking

Y	Value Marking on black side
Nil	No marking ★

Resistance Tolerance

J	±5%
K	±10%
O	Jumper

Nominal Resistance Value

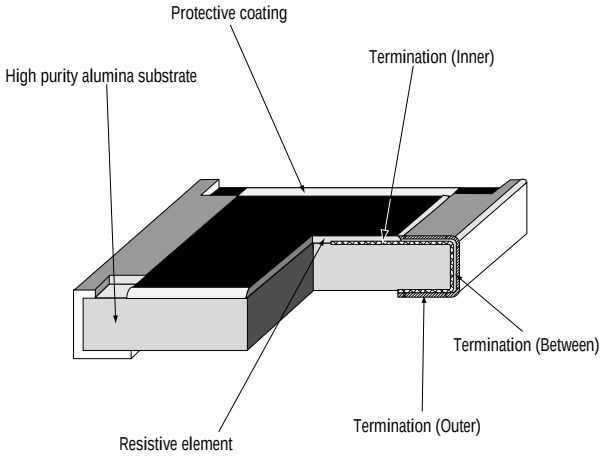
The first two digits are significant figures of resistance value and the third one denotes the number of zeros following. Jumper is expressed by R00.

Packaging

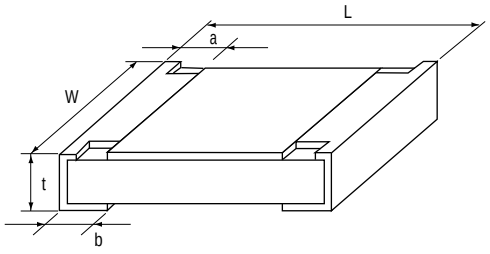
V	Std. taped and reel
U	Plastic embossed tape and reel
B	Bulk case
X	2mm pitch T. and R. (Only 2G, 3G type)

★ When omitted, the remainding part numbers shall be moved up respectively.

Construction



Dimensions in mm (not to scale)



Part No.	Dimensions L	W	a	b	t	Net Weight (1000 pcs.)
ERJ2GE	$1.00^{\pm0.05}$	$0.50^{\pm0.05}$	$0.20^{\pm0.10}$	$0.25^{\pm0.05}$	$0.35^{\pm0.05}$	0.8 g
ERJ3GS	$1.60^{\pm0.15}$	$0.80^{+0.05}_{-0.05}$	$0.30^{\pm0.20}$	$0.30^{\pm0.15}$	$0.45^{\pm0.10}$	2 g
ERJ6GE	$2.00^{\pm0.20}$	$1.25^{\pm0.10}$	$0.40^{\pm0.20}$	$0.40^{\pm0.20}$	$0.60^{\pm0.10}$	4 g
ERJ8G3	$3.20^{\pm0.20}$	$1.60^{+0.10}_{-0.05}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	10 g
ERJ14	$3.20^{\pm0.20}$	$2.50^{+0.10}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	16 g
ERJ12	$4.50^{\pm0.20}$	$3.20^{+0.10}$	$0.50^{\pm0.20}$	$0.50^{\pm0.20}$	$0.60^{\pm0.10}$	27 g
ERJ1W	$6.40^{\pm0.20}$	$3.20^{+0.10}$	$0.65^{\pm0.20}$	$1.30^{\pm0.20}$	$1.10^{\pm0.10}$	79 g

■ Ratings

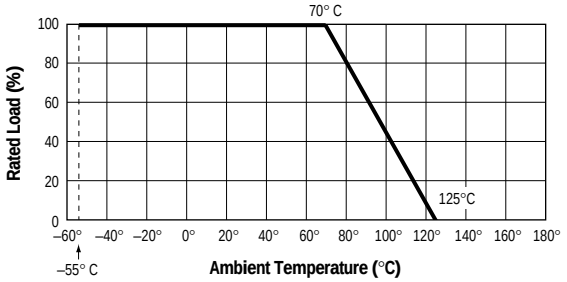
	Power Rating at 70°C	Maximum RCWV*	Maximum Overload Voltage▲	Resistance Tolerance●	Resistance Range (Ω) min.	Resistance Range (Ω) max.	T.C.R. (ppm/°C)	Standard Resistance Values
ERJ2G	1/16W	50V	100V	±5	1.0	2.2 M		E-24
ERJ3G	1/16W	50V	100V	±5	1.0	10 M	<10Ω	E-24
	(1/10W)◆						–100 to	E-12
ERJ6G	1/10W	150V	200V	±5	1.0	10 M	600	E-24
	(1/8W)◆	150V	200V	±10	0.47	10 M		E-12
ERJ8G	1/8W	200V	400V	±5	1.0	10 M	100Ω to	E-24
	(1/4W)◆			±10	0.39	10 M	1 MΩ	E-12
ERJ14	1/4W	200V	400V	±5	1.0	10 M	±200	E-24
				±10	1.0	1.0 M		E-12
ERJ12	1/2W	200V	400V	±5	1.0	10 M	1MΩ<	E-24
				±10	1.0	1.0 M	–400 to	E-12
ERJ1W	1W	250V	500V	±5	10	1.0 M	+150	E-24
				±10	1.0	1.0 M		E-12

		Rated Current	Max. Overload Current
Jumper	2G • 3G	1.0A	2A
	6G • 8G • 14 • 12	2.0A	4A
	1W	2.5A	5A

* Rated Continuous Working Voltage (RCWV) shall be determined from RCWV = $\sqrt{\text{Power Rating x Resistance Value}}$, or max. RCWV listed above, whichever less.
◆ Available for reduction of load of pulse characteristics (RCWV x 2.5 RCW x 2.0, R≥1.1 kΩ)
● Available for ±1% or ±2% of resistance tolerance.
▲ Short-time Overload Test Voltage (SOTV) shall be determined from SOTV + 2.5 x Power Rating or max. Overload Voltage listed above whichever less.

Power Derating Curve

For resistors operated in ambient temperature above 70°C, power rating shall be derated in accordance with the figure to the right.

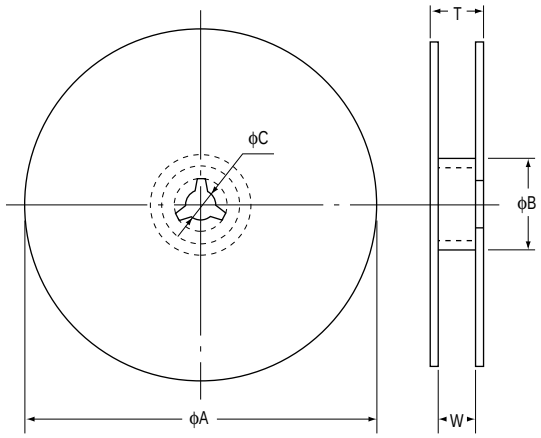


■ Packing Methods

Type	Thickness	Paper Taping (4mm pitch)	Embossed Taping (4mm pitch)	Bulk Case
ERJ2G	0.35	10,000 (2mm pitch)		50,000 pcs./case
ERJ3G	0.45	10,000 (2mm pitch)* 5,000, 10,000*, 20,000*		25,000 pcs./case
ERJ6G	0.60	5,000, 10,000*, 20,000*		10,000 pcs./case
ERJ8G	0.60	5,000, 10,000*, 20,000*		
ERJ14	0.60	5,000 pcs./reel		
ERJ12	0.60	5,000 pcs./reel (4mm pitch)		
ERJ1W	1.10	3,000 pcs./reel (4mm pitch)		

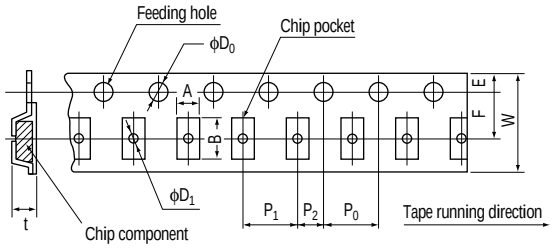
■ Packaging Methods *(cont'd)*

Taping Reel



	Dimensions				
	φA	φB	φC	W	T
2G, 3G, 6G, 8G, 14	$180.0^{+0}_{-3.0}$	60 min.	$13.0^{\pm1.0}$	$10.0^{\pm1.0}$	$12.0^{\pm2.0}$
12, 1W				$14.0^{\pm1.0}$	$16.0^{\pm2.0}$

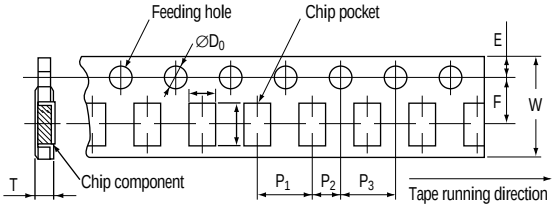
Embossed Taping



	Dimensions					
Type	A	B	W	F	E	P_1
14	$2.80^{\pm0.05}$	$3.50^{\pm0.20}$	$8.00^{\pm0.30}$	$3.50^{\pm0.05}$	$1.75^{\pm0.10}$	$4.00^{\pm0.10}$
12	$3.50^{\pm0.20}$	$4.80^{\pm0.20}$	$12.0^{\pm0.30}$	$5.50^{\pm0.05}$		$8.00^{\pm0.20}$
1W	$3.60^{\pm0.20}$	$6.90^{\pm0.20}$				$8.00^{\pm0.20}$

Type	P_2	P_0	φD_0	t	φD_1
14	$2.00^{\pm0.10}$	$4.00^{\pm0.10}$	$1.50^{\pm0.10}$	$1.00^{\pm0.10}$	1.00
12					1.50 min.
1W				$1.60^{\pm0.10}$	

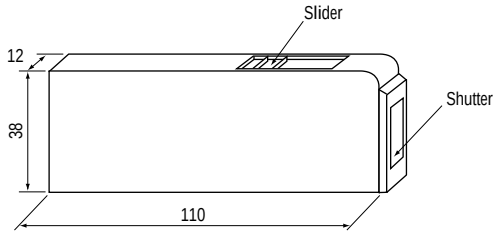
Paper Taping



	Dimensions				
Type	A	B	W	F	E
2G	$0.70^{\pm0.05}$	$1.20^{\pm0.20}$	$8.00^{\pm0.20}$	$3.50^{\pm0.05}$	$1.75^{\pm0.10}$
3G	$1.10^{\pm0.10}$	$1.90^{\pm0.10}$			
6G	$1.60^{\pm0.15}$	$2.40^{\pm0.20}$			
8G	$1.90^{\pm0.15}$	$3.50^{\pm0.20}$			

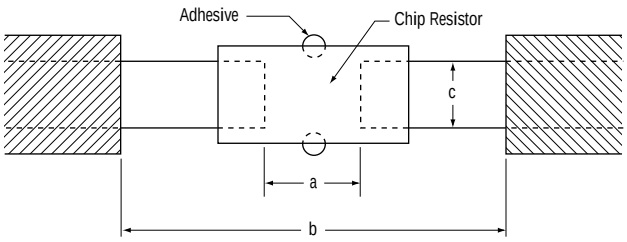
Type	P_1	P_2	P_0	φD_0	t_2
2G	$2.00^{\pm0.10}$	$2.00^{\pm0.05}$	$4.00^{\pm0.10}$	$1.50^{\pm0.10}$	$0.45^{\pm0.05}$
3G	$4.00^{\pm0.10}$				$0.64^{\pm0.05}$
6G					$0.84^{\pm0.05}$
8G					$0.84^{\pm0.05}$

Bulk Case



■ Safety Precautions

In the case of flow soldering, the land width must be smaller than the Chip Resistor width to control the solder amount properly. Generally, the land width should be chip resistor width (W) 0.7 to 0.8 times of the width of chip resistor. In the case of reflow soldering, solder amount can be adjusted, therefore the land width should be set to 1.0 to 1.3 times chip resistor width (W).



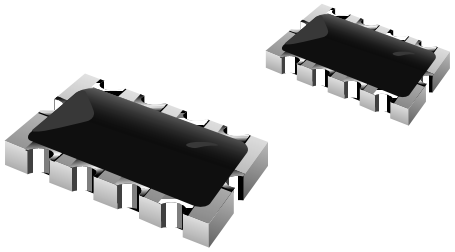
	Dimensions		
Part No.	**a**	**b**	**c**
ERJ2G	0.5 to 0.6	1.4 to 1.6	0.4 to 0.6
ERJ3G	0.7 to 0.9	2.0 to 2.2	0.8 to 1.0
ERJ6G	1.0 to 1.4	3.2 to 3.8	0.9 to 1.4
ERJ8G	2.0 to 2.4	4.4 to 5.0	1.2 to 1.8
ERJ14	2.0 to 2.4	4.4 to 5.0	1.8 to 2.8
ERJ12	3.3 to 3.7	5.7 to 6.5	2.3 to 3.5
ERJ1W	3.6 to 4.0	7.6 to 8.6	2.3 to 3.5

1. If transient load (heavy load in a short time) like pulse is expected to be aplied, carry out evaluation and confirmation tset with the resistors actually mounted on your own board.

   When the load of more than rated power is applied under the load condition at a steady rate, it may impair performance and/or reliability of resistor. Never exceed the rated power.
2. Chlorine-type or other high-activity flux is not recommended as the residue may affect performmance or reliability of resistors.
3. When soldering with soldering iron, never tough the body of the chip resistor with the tip of the soldering iron. When using a soldering iron with a tip at high temperature, solder for a time as short as possible (three seconds or less up to 350°C.)
4. Avoid physical shock to the resistor and nipping of the resistor with hard tool (a pair of pliers or tweezers) as it may damage protective film or the body of resistor and may affect resistor's performance.

Chip Resistor Array

Series: EXB2
EXBV
EXBS



■ Features

- High density
  - 2 resistors in 1.0mm x 1.0mm size (24V)
  - 2 resistors in 1.6mm x 1.6mm size (V4V)
  - 4 resistors in 3.2mm x 1.6mm size (V8V)
  - 4 resistors in 5.08mm x 2.2mm size (S8V)
- Improvement of placement efficiency—Placement efficiency of chip resistor array is two to four times that of flat type chip resistor

■ Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11
E	X	B	V	8	V	4	7	2	J	
Product Code			Chip Resistor Array	No. of Terminals	Schematics	Resistance Value			Resistance Tolerance	Packaging

Product Code: Thick Film Resistor Networks

Chip Resistor Array

2	1005 array
V	1608 array
S	2012 array

No. of Terminals

4	4 pins
8	8 pins

Schematics

V	Isolated type

Resistance Value: The first two digits are significant figures of resistance value and the third one denotes the number of zeros following. Jumper is expressed by R00.

Example: 222: 2.2 kΩ

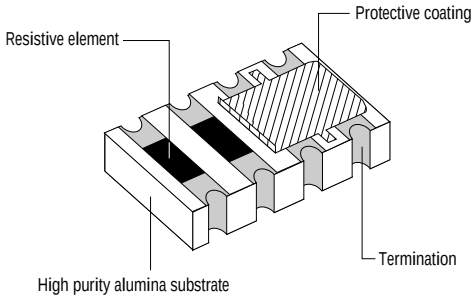
Resistance Tolerance

G	±2%
J	±5%
O	Jumper

Packaging

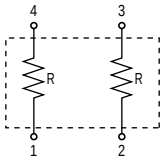
Nil	Embossed taping (Only S8 type)
V	Paper taping
S	2mm pitch Tape and reel (Only 24 type)

■ Construction

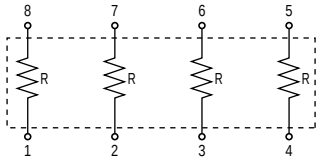


■ Schematics—Isolated Type

24V, V4V
2 resistors

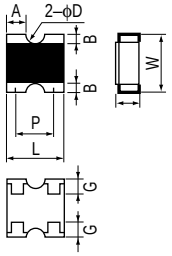


V8V, S8V
4 resistors

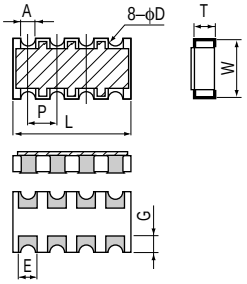


■ Dimensions in mm (not to scale)

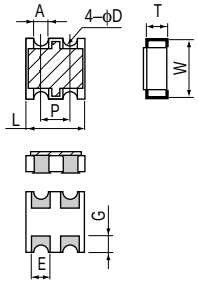
24V



V8V, S8V



V4V



Type	Dimensions								
	L	W	T	A	B	φD	P	E	G
24V	$1.00^{\pm0.05}$	$0.35^{\pm0.05}$	$0.33^{\pm0.05}$	$0.33^{\pm0.10}$	$0.15^{\pm0.05}$	$0.34^{\pm0.05}$	$0.65^{\pm0.10}$	—	$0.25^{\pm0.05}$
V4V	$1.60^{\pm0.20}_{-0.10}$	$1.6^{\pm0.20}_{-0.10}$	$0.60^{\pm0.10}$	$0.60^{\pm0.10}$	$0.30^{\pm0.15}$	(0.3)	$0.80^{\pm0.10}$	$0.45^{\pm0.15}$	$0.40^{\pm0.15}$
V8V	$3.20^{\pm0.20}_{-0.10}$								
S8V	$5.08^{\pm0.20}_{-0.10}$	$2.20^{\pm0.20}_{-0.10}$	$0.70^{\pm0.10}$	$0.80^{\pm0.10}$	$0.50^{\pm0.15}$	(0.5)	$1.27^{\pm0.10}$	$0.70^{\pm0.20}$	$0.55^{\pm0.15}$

( ) Reference

■ Ratings

Resistance range	10Ω to 1Ω: E24 series	
Resistance tolerance	**2**	J: ± 5%
	V	G: ± 2%, J: ±5%
	S	G: ±2%, J: ±5%
Number of terminals	**24V**	4 terminal
	4V	4 terminal
	8V	8 terminal
Number of resistors	**2, V**	2 resistors
	8V	4 resistors
Power rating at 70°C	**2, V**	1/16 w/ element
	S	1/10 w/ element

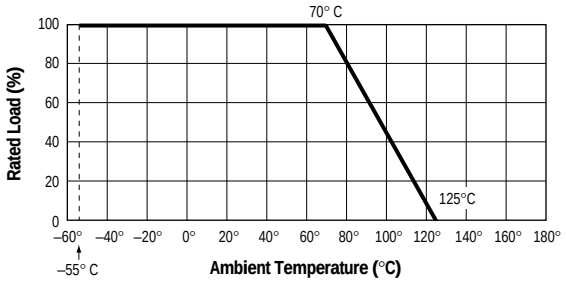
Max. rated continuous working voltage*	**2, V**	50V
	S	100V
Max. overload voltage	**2, V**	100 V
	S	200V
Temperature characteristic range		±200 ppm/°C
Operating temperature range		–55°C to 125°C
Storage temperature range		–55°C to 125°C
Jumper Array: Rated current		1 A, (24, 8V, 4V) 2A (S8)
Jumper Array: Max. overload current		2A (24, 8V, 4V) 4A (S8)

* Rated Continuous Working Voltage (RCWV) shall be determined from RCWV = $\sqrt{\text{Power Rating x Resistance Value}}$, or max. RCWV listed above, whichever is less.

** Short-time Overload Test voltage (SOTV) shall be determined from SOTV = 2.5 x Power Rating or max. Overload Voltage listed above, whichever less.

Power Derating Curve

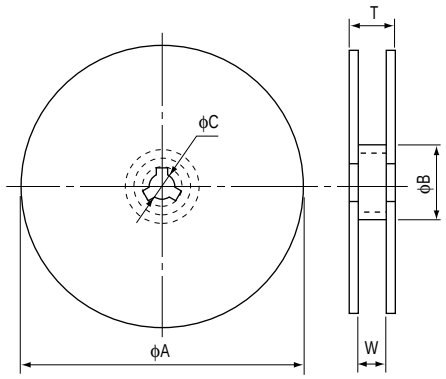
For resistors operated in ambient temperature above 70°C, power rating shall be derated in accordance with the right figure.



■ Packaging Methods—Standard Quantity

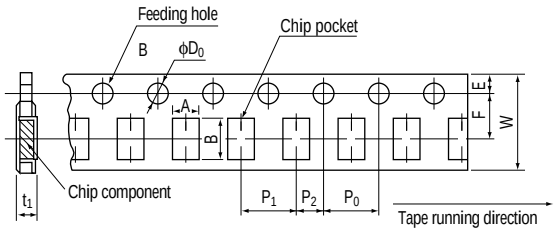
Type	Thickness	Weight/1000 pcs.	Paper Taping	Embossed Taping
EXB2	0.35 ± 0.05mm	1.2g	10,000 pcs./reel	—
EXBV	0.6 ± 0.1mm	V4: 5G V8: 10g	5,000 pcs./reel	—
EXBS	0.7 ± 0.1mm	30 g	—	2,500 pcs./reel

Paper Taping Reel



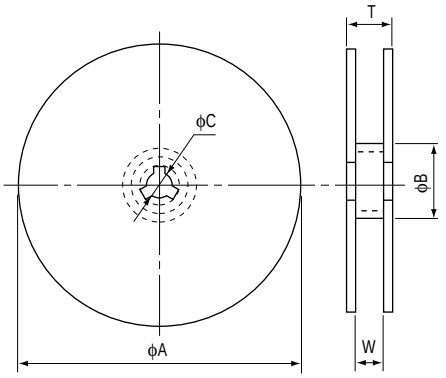
Type	Dimensions				
	ϕA	ϕB	ϕC	W	T
2	180.0 $^{0}_{-3.0}$	60.0 min.	13.0 $^{\pm1.0}$		
V				10.0 $^{\pm1.0}$	12.0 $^{\pm2.0}$

Paper Taping



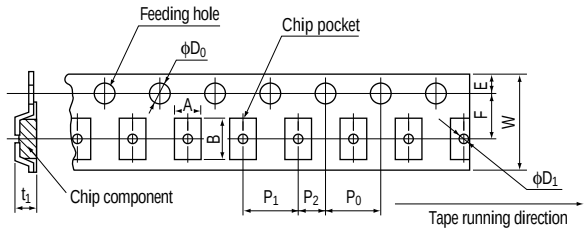
Type	Dimensions				
	ϕA	ϕB	W	F	E
24V	1.20 $^{\pm0.05}$	1.20 $^{\pm0.05}$			
V4V	1.95 $^{\pm0.15}$	1.95 $^{\pm0.20}$	8.00 $^{\pm0.20}$	3.50 $^{\pm0.05}$	1.75 $^{\pm0.10}$
V8V	2.00 $^{\pm0.15}$	3.60 $^{\pm0.20}$			
Type	**P 1**	**P 2**	**ϕD0**	**t 2**	**ϕD1**
24V	2.00 $^{\pm0.10}$	2.00 $^{\pm0.05}$	4.00 $^{\pm0.10}$	1.50 $^{+0.10}_{0}$	0.45 $^{\pm0.05}$
V4V	4.00 $^{\pm0.10}$				0.84 $^{\pm0.05}$
V8V					

Embossed Taping Reel



Type	Dimensions				
	ϕA	ϕB	ϕC	W	T
S	180.0 $^{0}_{-3.0}$	50.0 min.	13.0 $^{\pm0.5}$	14.0 $^{\pm1.5}$	20.5 max.

Embossed Taping

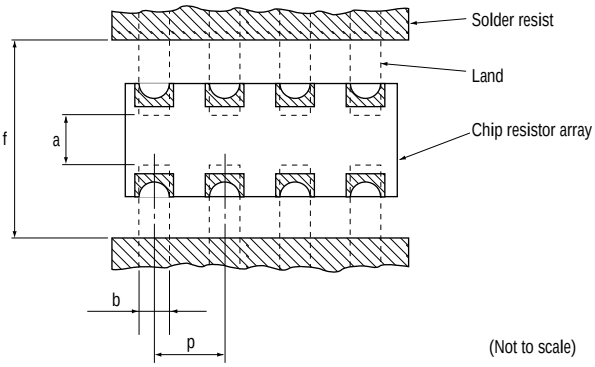


Type	Dimensions					
	A	B	W	F	E	P 0
S8V	2.80 $^{\pm0.20}$	5.70 $^{\pm0.20}$	12.00 $^{\pm0.30}$	5.50 $^{\pm0.05}$	1.75 $^{\pm0.10}$	4.00 $^{\pm0.10}$
Type	**P 1**	**P 2**	**ϕD0**	**t 2**	**ϕD0**	
S8V	4.00 $^{\pm0.10}$	2.00 $^{\pm0.05}$	1.50 $^{+0.10}_{0}$	1.60 max.	1.50 $^{+0.10}_{0}$	

■ Safety Precautions

1. Land pattern design. Recommendable land pattern design for Network chip is as shown at the right.

Type	Dimensions (in mm.)			
	a	b	p	f
24V	0.5	0.5	0.65	1.5
V8V	0.7 to 0 .9	0.4 to 0.45	0.80	2.0 to 2.2
S8V	1.0 to 1.2	0.5 to 0.75	1.27	3.2 to 3.8

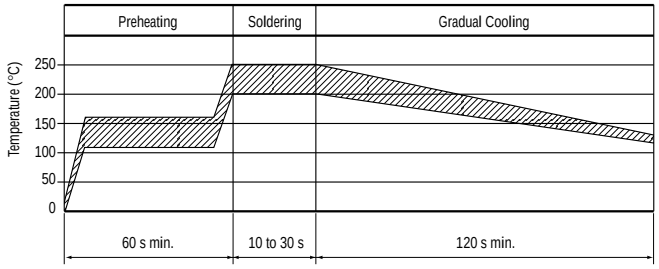


■ Safety Precautions *(cont'd)*

2. **Component placement.** Take measure against mechanical stress during and after mounting so as not to damage the termination and protective coating. Misplacement of components on the land pattern may cause solder bridge problem.
3. **Soldering.** Precaution and recommendations are described below.

   (a) Soldering iron. Soldering iron tip shall not touch the protective coating of the part. Solder as quick as possible (within three seconds) when the temperature of the soldering iron tip is over 280°C.

   (b) Reflow soldering: Recommendable reflow soldering is shown below.



   (c) Flow soldering: Ask us when you use chip resistor with flow soldering method.

4. **Cleaning.** Recommended cleaning method is shown below.

	Cleaning condition	
Solvent	**Dipping**	**Ultrasonic Wave Washing**
Isopropyl Alcohol	5 min. max.	1 min. max. Power: 20 W/L Frequency: 10 to 100 kHz

5. If transient load (heavy load in a short time) like pulse is expected to be applied, carry out evaluation and confirmation test with the resistors actually mounted on your own board. When the load of more than rated power is applied under the load condition at steady state, it may impair performance and/or reliability of resistor. Never exceed the rated power.
6. Chlorine-type or other high-activity flux is not recommended as the residue may affect performance or reliability of resistors.
7. When soldering with soldering iron, never touch the body of the chip resistor with a tip of the soldering iron. When using a soldering iron with a tip at high temperature, solder for a time as short as possible (three seconds or less up to 350°C).
8. Avoid physical shock to the resistor and nipping of the resistor with a hard tool (a pair of pliers or tweezers) as it may damage protective film or the body of resistor and may affect resistor's performance.
9. Do not use the product in dewy atmosphere.

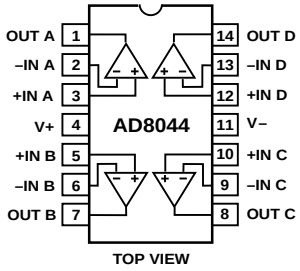
Quad 150 MHz Rail-to-Rail Amplifier

AD8044

FEATURES
Fully Specified for +3 V, +5 V, and ±5 V Supplies
Output Swings Rail to Rail
Input Voltage Range Extends 200 mV Below Ground
No Phase Reversal with Inputs 1 V Beyond Supplies
Low Power of 2.75 mA/Amp
High Speed and Fast Settling on +5 V:
150 MHz –3 dB Bandwidth (G = +1)
170 V/μs Slew Rate
45 ns Settling Time to 0.1%
Good Video Specifications (R_L = 150 Ω, G = +2)
Gain Flatness of 0.1 dB to 12 MHz
0.06% Differential Gain Error
0.15° Differential Phase Error
Low Distortion
–58 dBc Worst Harmonic @ 5 MHz
Outstanding Load Drive Capability
Drives 50 mA 0.5 V from Supply Rails
Cap Load Drive of 45 pF

APPLICATIONS
Active Filters
Power Sensitive High Speed Systems
Video Switchers
Distribution Amplifiers
A/D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)

CONNECTION DIAGRAM
14-Pin Plastic Mini-DIP and SOIC



TOP VIEW

PRODUCT DESCRIPTION

The AD8044 is a quad low power, voltage feedback, high speed amplifier designed to operate on +3 V, +5 V or ±5 V supplies. It has true single-supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

The output voltage swing extends to within 25 mV of each rail, providing the maximum output dynamic range. Additionally, it features gain flatness of 0.1 dB to 12 MHz while offering differential gain and phase error of 0.05% and 0.25° on a single +5 V supply. This makes the AD8044 ideal for video electronics such as cameras, video switchers or any high speed portable equipment. The AD8044's low distortion and fast settling make it ideal for active filter applications.

The AD8044 offers low power supply current of 13 mA max and can run on a single +3 V power supply. These features are ideally suited for portable and battery powered applications where size and power are critical.

The wide bandwidth of 150 MHz along with 170 V/μs of slew rate on a single +5 V supply make the AD8044 useful in many general purpose, high speed applications where dual power supplies of up to ±6 V and single supplies from +3 V to +12 V are needed. The AD8044 is available in 14-pin plastic DIP and SOIC.

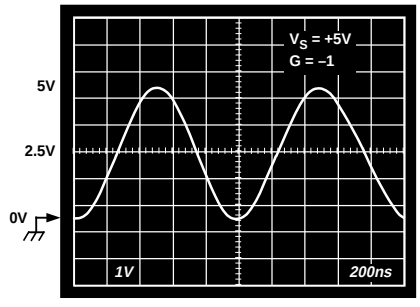


Figure 1. Output Swing: Gain = –1, V_S = +5 V

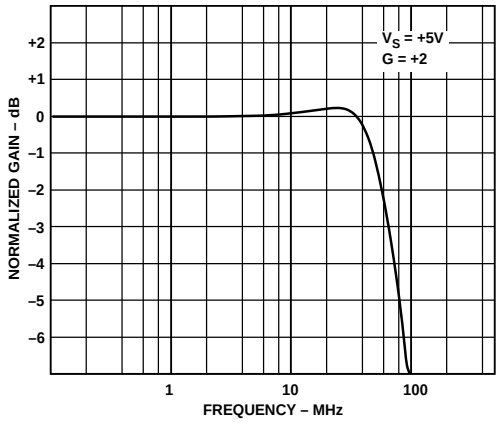


Figure 2. Frequency Response: Gain = +2, V_S = +5 V

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD8044—SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	AD8044A Typ	AD8044A Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	130	150		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		12		MHz
Slew Rate	G = –1, V_O = 2 V Step	140	170		V/µs
Full Power Response	V_O = 2 V p-p		26		MHz
Settling Time to 1%	G = –1, V_O = 2 V Step		30		ns
Settling Time to 0.1%			40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–75		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		850		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.04		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.22		Degrees
Crosstalk	f = 5 MHz, R_L = 1 kΩ, G = +2		60		dB
DC PERFORMANCE					
Input Offset Voltage			1.0	4	mV
	T_{MIN}–T_{MAX}			6.2	mV
Offset Drift			8		µV/°C
Input Bias Current			2	3.0	µA
	T_{MIN}–T_{MAX}			4	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	86	94		dB
	T_{MIN}–T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–0.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	80	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			0.03 to 4.975		V
R_L = 1 kΩ		0.17 to 4.83	0.075 to 4.91		V
R_L = 50 Ω		1.4 to 3.6	0.68 to 4.1		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = 0.5 V to 4.5 V		30		mA
Short Circuit Current	Sourcing		50		mA
	Sinking		90		mA
Capacitive Load Drive	G = +2		40		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			11	13	mA
Power Supply Rejection Ratio	V_S = 0, +5 V, ±1 V	72	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = +25°C, V_S = +3 V, R_L = 2 kΩ to 1.5 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	120	135		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		10		MHz
Slew Rate	G = –1, V_O = 2 V Step	125	150		V/µs
Full Power Response	V_O = 2 V p-p		22		MHz
Settling Time to 1%	G = –1, V_O = 2 V Step		35		ns
Settling Time to 0.1%			55		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = –1, R_L = 100 Ω		–54		dB
Input Voltage Noise	f = 10 kHz		16		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz		600		$fA/\sqrt{Hz}$
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 1.5 V, Input V_{CM} = 0.5 V		0.13		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 1.5 V, Input V_{CM} = 0.5 V		0.3		Degrees
Crosstalk	f = 5 MHz		60		dB
DC PERFORMANCE					
Input Offset Voltage			1.5	4	mV
	T_{MIN}–T_{MAX}			6.2	mV
Offset Drift			8		µV/°C
Input Bias Current			2	3.5	µA
	T_{MIN}–T_{MAX}			3.5	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	86	92		dB
	T_{MIN}–T_{MAX}		89		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–0.2 to 2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	76	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			0.025 to 2.98		V
R_L = 1 kΩ		0.15 to 2.85	0.06 to 2.93		V
R_L = 50 Ω		1.0 to 2.0	0.4 to 2.4		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = 0.5 V to 2.5 V		25		mA
Short Circuit Current	Sourcing		35		mA
	Sinking		50		mA
Capacitive Load Drive	G = +2		35		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			10.5	12.2	mA
Power Supply Rejection Ratio	V_S = 0, +3 V, ±0.5 V	72	80		dB
OPERATING TEMPERATURE RANGE		0		+70	°C

Specifications subject to change without notice.

AD8044—SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 2 kΩ to 0 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	AD8044A Typ	AD8044A Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	140	160		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		15		MHz
Slew Rate	G = –1, V_O = 2 V Step	150	190		V/µs
Full Power Response	V_O = 2 V p-p		29		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		30		ns
Settling Time to 0.01%			40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–77		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		900		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω		0.06		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω		0.15		Degrees
Crosstalk	f = 5 MHz		60		dB
DC PERFORMANCE					
Input Offset Voltage			1.4	4.5	mV
	T_{MIN}–T_{MAX}			6.8	mV
Offset Drift			10		µV/°C
Input Bias Current			2	3.5	µA
	T_{MIN}–T_{MAX}			3.5	µA
Input Offset Current			0.2	0.6	µA
Open-Loop Gain	R_L = 1 kΩ	90	96		dB
	T_{MIN}–T_{MAX}		95		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–5.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = –5 V to 3.5 V	76	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			–4.97 to +4.97		V
R_L = 1 kΩ		–4.75 to +4.75	–4.85 to +4.85		V
R_L = 50 Ω		–1.5 to +1.5	–2.5 to +2.5		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = –4.5 V to +4.5 V		30		mA
Short Circuit Current	Sourcing		60		mA
	Sinking		110		mA
Capacitive Load Drive	G = +2		40		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			11.5	13.5	mA
Power Supply Rejection Ratio	V_S = –5, +5 V, ±1 V	72	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +12.6 V
Internal Power Dissipation[2]
  Plastic Package (N) . . . . . 1.6 Watts
  Small Outline Package (R) . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±3.4 V
Output Short Circuit Duration
  . . . . . Observe Power Derating Curves
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for the device in free air:
14-Pin Plastic Package: θ_{JA} = 75°C/Watt
14-Pin SOIC Package: θ_{JA} = 120°C/Watt.

ORDERING GUIDE

Model	Supply Voltage	Temperature Range	Package Description
AD8044AN	+5, ±5	–40°C to +85°C	14-Pin Plastic DIP (N-14)
AD8044AN	+3	0°C to +70°C	14-Pin Plastic DIP (N-14)
AD8044AR	+5, ±5	–40°C to +85°C	14-Pin Plastic SOIC (R-14)
AD8044AR	+3	0°C to +70°C	14-Pin Plastic SOIC (R-14)
AD8044AR-REEL			REEL-SOIC (R-14)

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8044 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8044 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

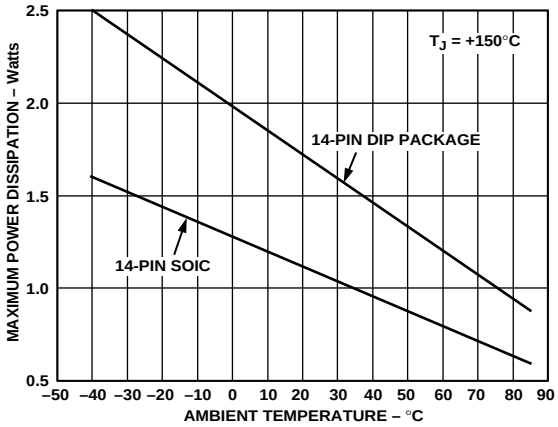


Figure 3. Maximum Power Dissipation vs. Temperature

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8044 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8044–Typical Performance Characteristics

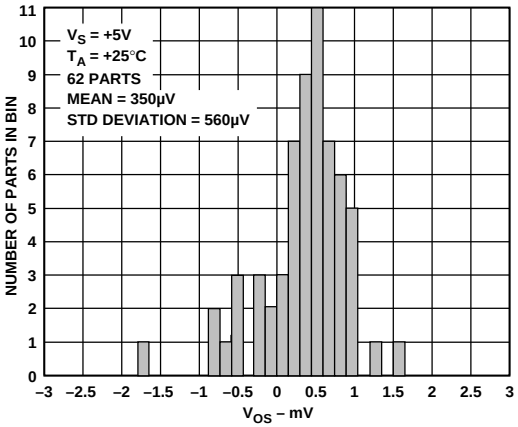


Figure 4. Typical Distribution of V_{OS}

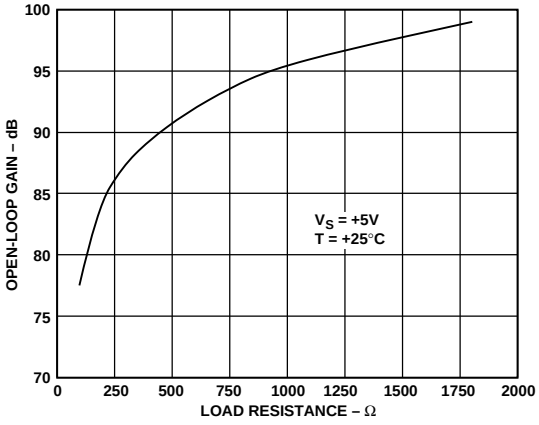


Figure 7. Open-Loop Gain vs. R_L to +2.5 V

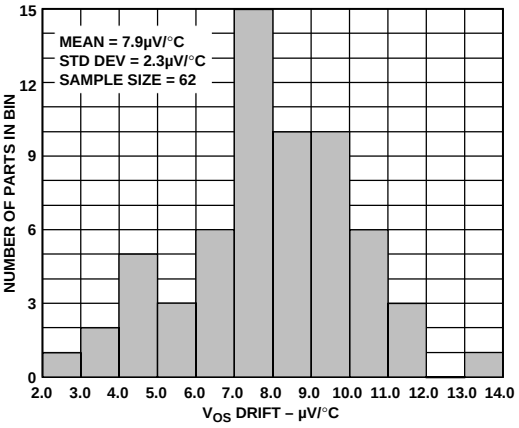


Figure 5. V_{OS} Drift Over –40°C to +85°C

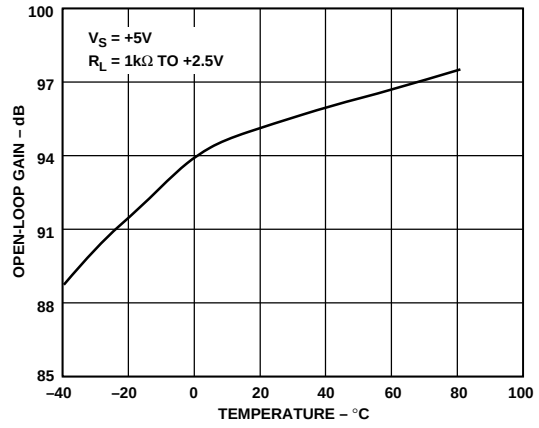


Figure 8. Open-Loop Gain vs. Temperature

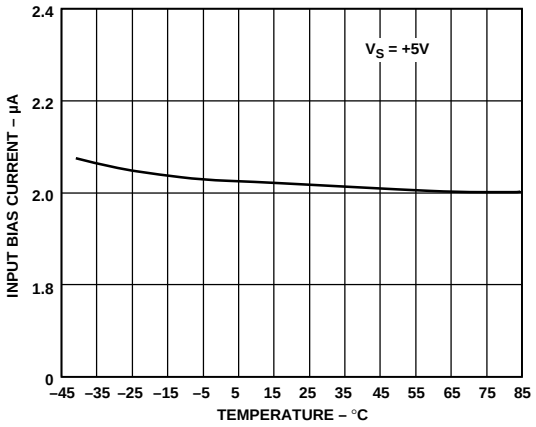


Figure 6. I_B vs. Temperature

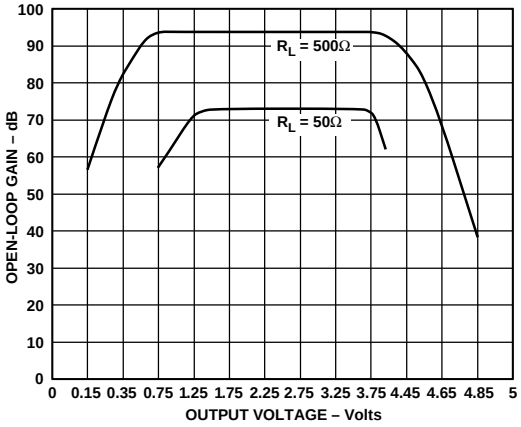


Figure 9. Open-Loop Gain vs. Output Voltage

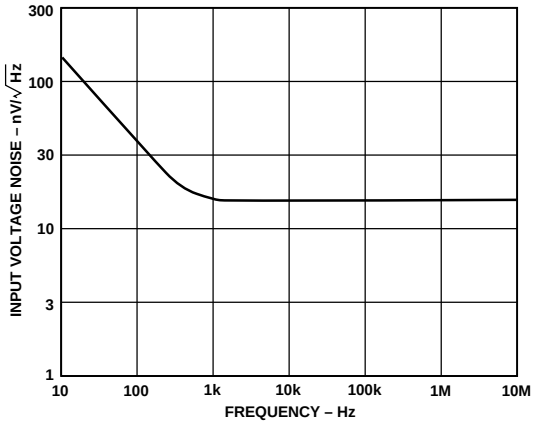


Figure 10. Input Voltage Noise vs. Frequency

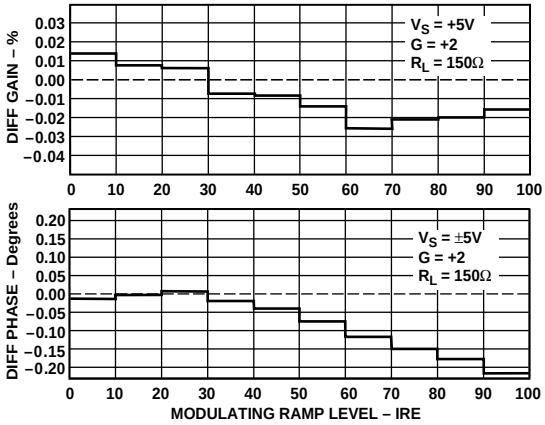


Figure 13. Differential Gain and Phase Errors

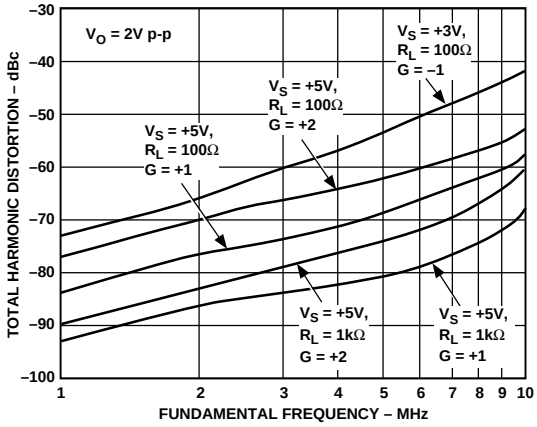


Figure 11. Total Harmonic Distortion

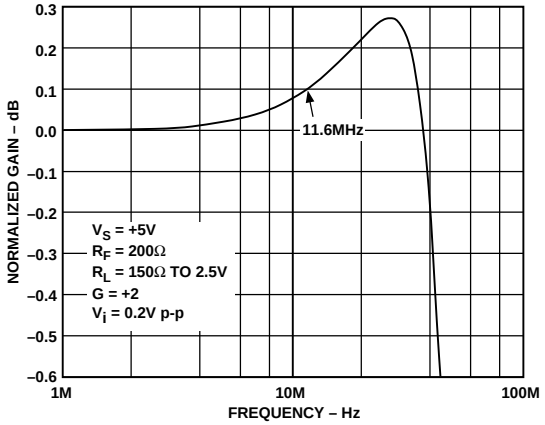


Figure 14. 0.1 dB Gain Flatness

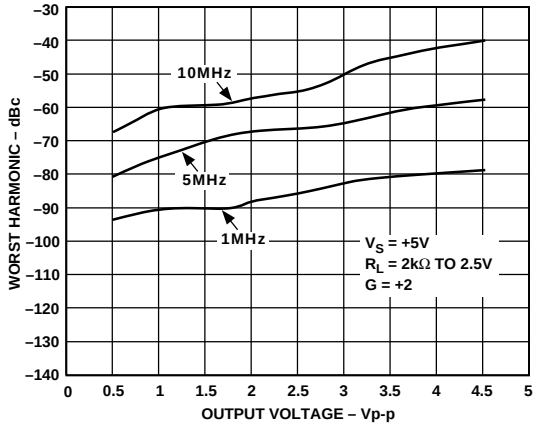


Figure 12. Worst Harmonic vs. Output Voltage

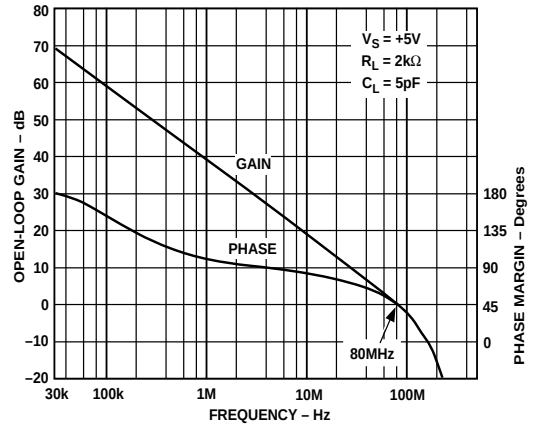


Figure 15. Open-Loop Gain and Phase Margin vs. Frequency

AD8044–Typical Performance Characteristics

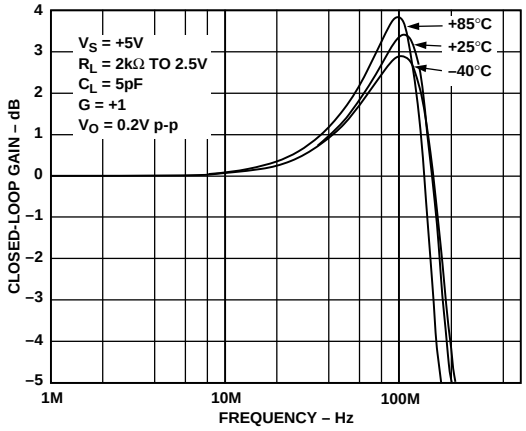


Figure 16. Closed-Loop Frequency Response vs. Temperature

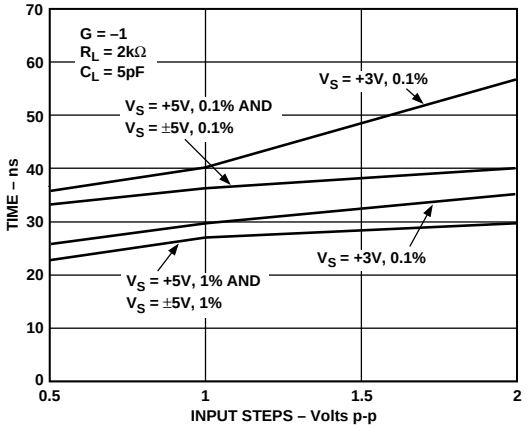


Figure 19. Settling Time vs. Input Step

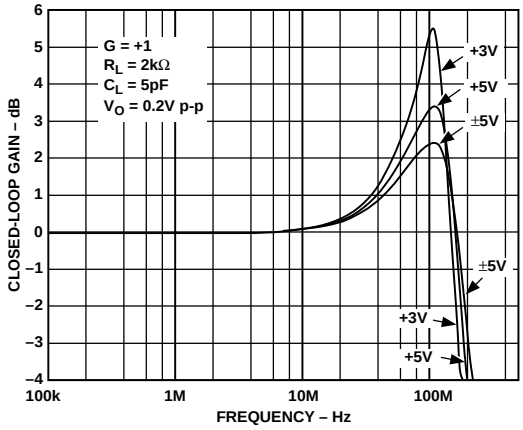


Figure 17. Closed-Loop Frequency Response vs. Supply

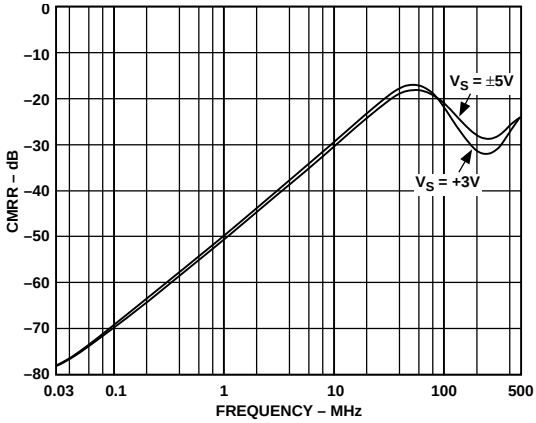


Figure 20. CMRR vs. Frequency

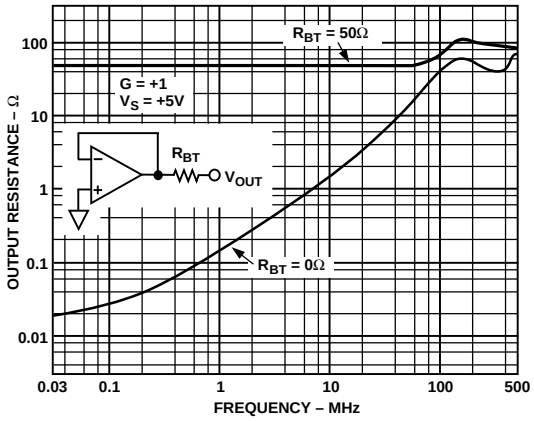


Figure 18. Output Resistance vs. Frequency

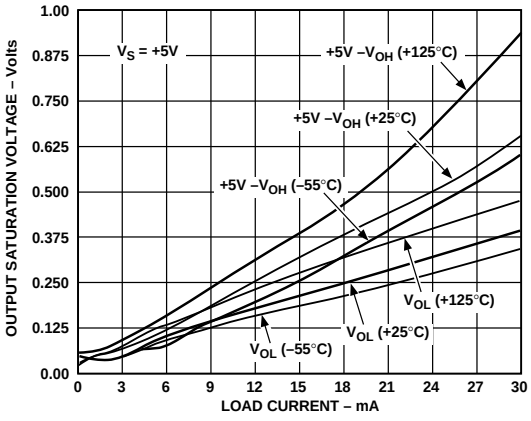


Figure 21. Output Saturation Voltage vs. Load Current

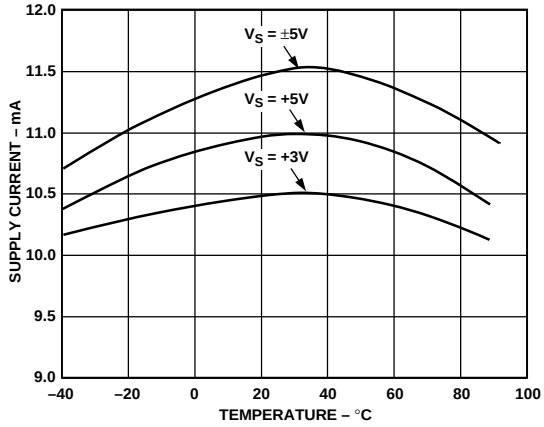


Figure 22. Supply Current vs. Temperature

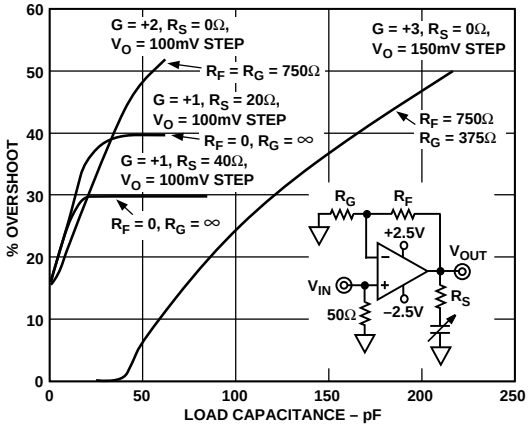


Figure 25. % Overshoot vs. Capacitive Load

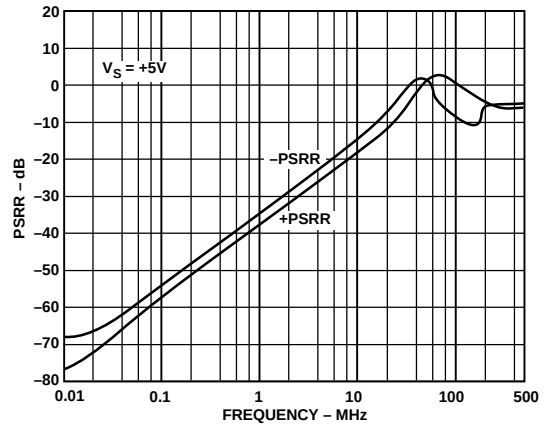


Figure 23. PSRR vs. Frequency

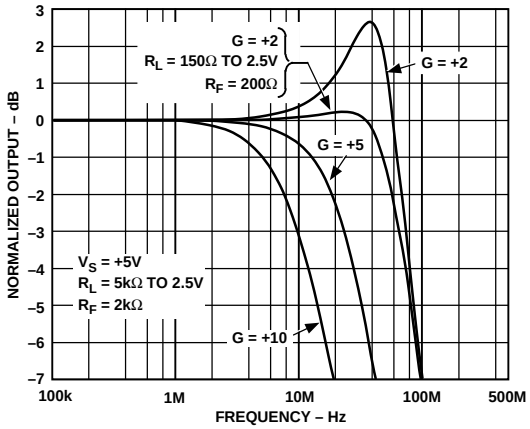


Figure 26. Frequency Response vs. Closed-Loop Gain

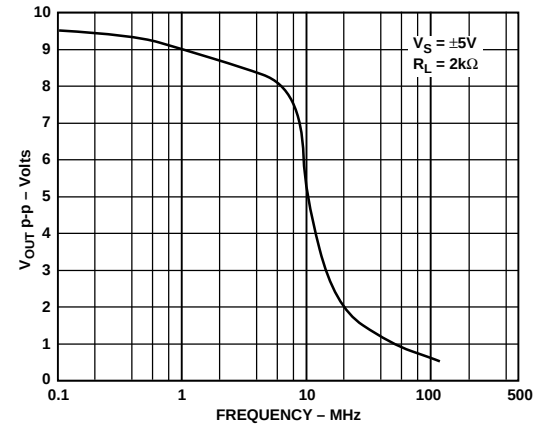


Figure 24. Output Voltage Swing vs. Frequency

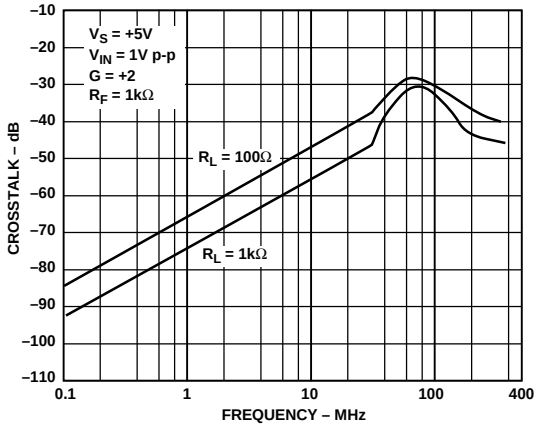
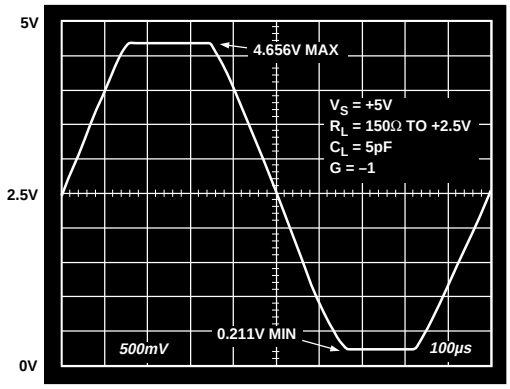
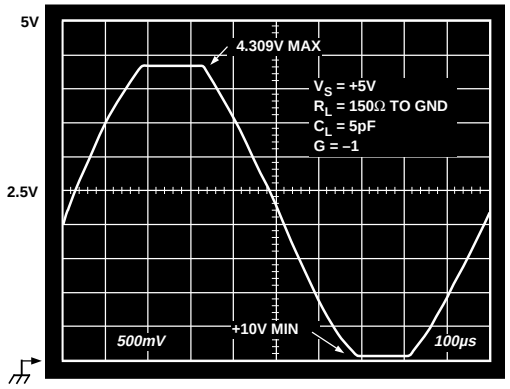


Figure 27. Crosstalk (Output to Output) vs. Frequency

AD8044–Typical Performance Characteristics



a.



b.

Figure 28. Output Swing vs. Load Reference Voltage, V_S = +5 V, G = –1

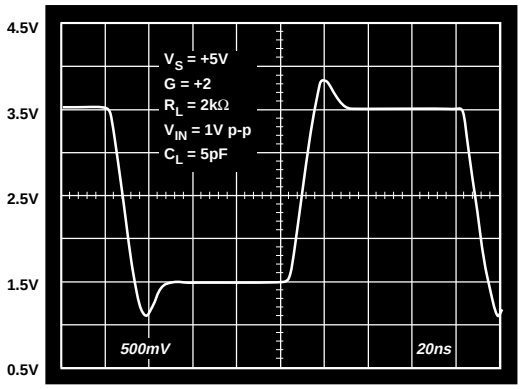


Figure 29. One Volt Step Response, V_S = +5 V, G = +2

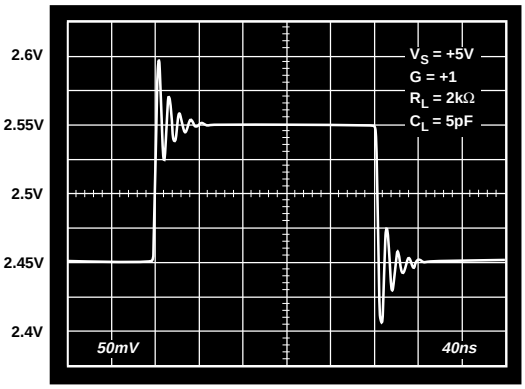


Figure 30. 100 mV Step Response, V_S = +5 V, G = +1

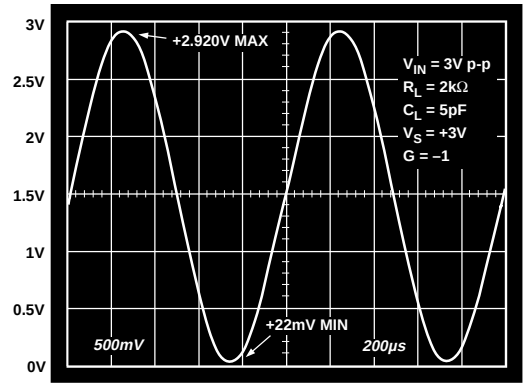


Figure 31. Output Swing, V_S = +3 V

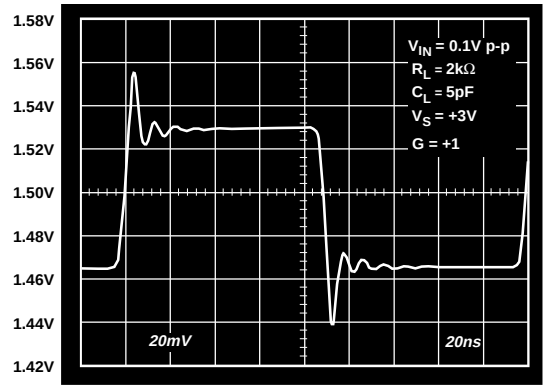


Figure 32. Step Response, G = +1, V_{IN} = 100 mV

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition. As shown in Figure 33, the AD8044 recovers within 50 ns from negative overdrive and within 25 ns from positive overdrive.

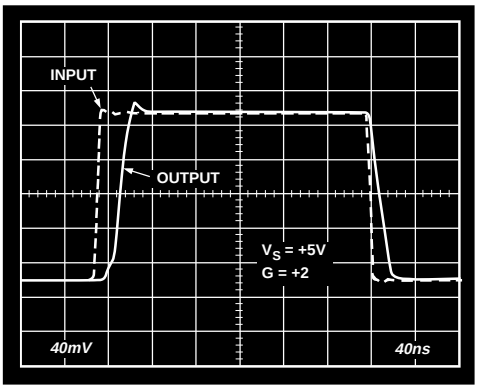


Figure 33. Overdrive Recovery

Circuit Description

The AD8044 is fabricated on Analog Devices' proprietary eXtra-Fast Complementary Bipolar (XFCB) process which enables the construction of PNP and NPN transistors with similar f_Ts in the 2 GHz–4 GHz region. The process is dielectrically isolated to eliminate the parasitic and latch-up problems caused by junction isolation. These features allow the construction of high frequency, low distortion amplifiers with low supply currents. This design uses a differential output input stage to maximize bandwidth and headroom (see Figure 34). The smaller signal swings required on the first stage outputs (nodes S1P, S1N) reduce the effect of nonlinear currents due to junction capacitances and improve the distortion performance. With this design harmonic distortion of better than –85 dB @ 1 MHz into 100 Ω with V_{OUT} = 2 V p-p (Gain = +2) on a single 5 volt supply is achieved.

The AD8044's rail to rail output range is provided by a complementary common-emitter output stage. High output drive capability is provided by injecting all output stage predriver currents directly into the bases of the output devices Q8 and Q36. Biasing of Q8 and Q36 is accomplished by I8 and I5, along with a common-mode feedback loop (not shown). This circuit topology allows the AD8044 to drive 50 mA of output current with the outputs within 0.5 V of the supply rails.

On the input side, the device can handle voltages from –0.2 V below the negative rail to within 1.2 V of the positive rail. Exceeding these values will not cause phase reversal; however, the input ESD devices will begin to conduct if the input voltages exceed the rails by greater than 0.5 V.

Output Impedance and Capacitance Drive

The AD8044's common-emitter output stage is very different than a typical emitter follower topology. Nonetheless, the amplifier's output impedance behaves the same way as traditional designs in a typical feedback application. The 110 dB loop gain reduces it to less than 0.1 Ω at low frequencies. At higher frequencies, the output impedance rises as the loop gain of the circuit drops (Figure 18). The output impedance eventually becomes capacitive due to integrator transistors C3 and C9.

Capacitive loads interact with the circuit output impedance to create an extra delay in the feedback path. This reduces circuit stability, and can cause unwanted ringing and oscillation. A given value of capacitance causes much less of an effect when the amplifier is used in a higher noise gain. This is illustrated in Figure 25, which plots the percent overshoot of the amplifier's step response when used in gains of +1, +2 and +3.

If greater phase margin is desired, a small resistor in series with the output can be used to isolate the loop from the effect of the load capacitance. Figure 25 shows the effect of this strategy with G = 4.

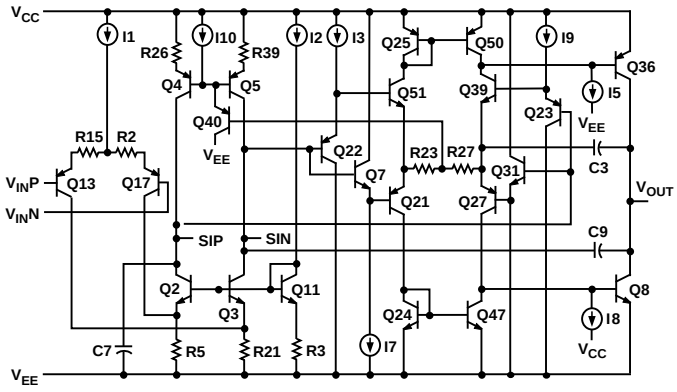


Figure 34. AD8044 Simplified Schematic

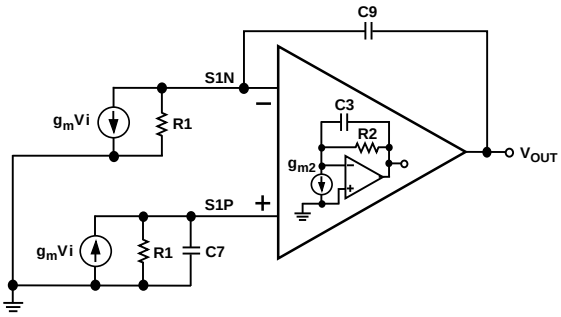


Figure 35. Small Signal Schematic

APPLICATIONS

RGB Buffer

The AD8044 can provide buffering of RGB signals that include ground while operating from a single +3 V or +5 V supply.

When driving two monitors from the same RGB video source it is necessary to provide an additional driver for one of the monitors to prevent the double termination situation that the second monitor presents. This has usually required a dual supply op amp, because the level of the input signal from the video driver goes all the way to ground during horizontal blanking. In single supply systems it can be a major inconvenience and expense to add an additional negative supply.

A single AD8044 can provide the necessary drive capability and yet does not require a negative supply in this application. Figure ?? is a schematic that uses three amplifiers out of a single AD8044 to provide buffering for a second monitor.

The source of the RGB signals is shown to be from a set of three current output DACs that are within a single supply graphics IC. This is typically the situation in most PCs and workstations which might use either a stand-alone triple DAC or the DACs could be integrated into a larger graphics chip.

During horizontal blanking, the current output from the DACs is turned off and the RGB outputs are pulled to ground by the termination resistors. If voltage sources were used for the RGB signals, then the termination resistors near the graphics IC would be in series and the rest of the circuit would remain the same. This is because a voltage source is an ac short circuit, so a series resistor is required to make the drive end of the line see 75 Ω to ac ground. On the other hand, a current source has a very high output impedance, so a shunt resistor is required to make the drive end of the line see 75 Ω to ground. In either case, the monitor terminates its end of the line with 75 Ω.

The circuit of Figure 36 shows minimum signal degradation when using a single supply for the AD8044. The circuit performs equally well on either a +3 V or +5 V supply.

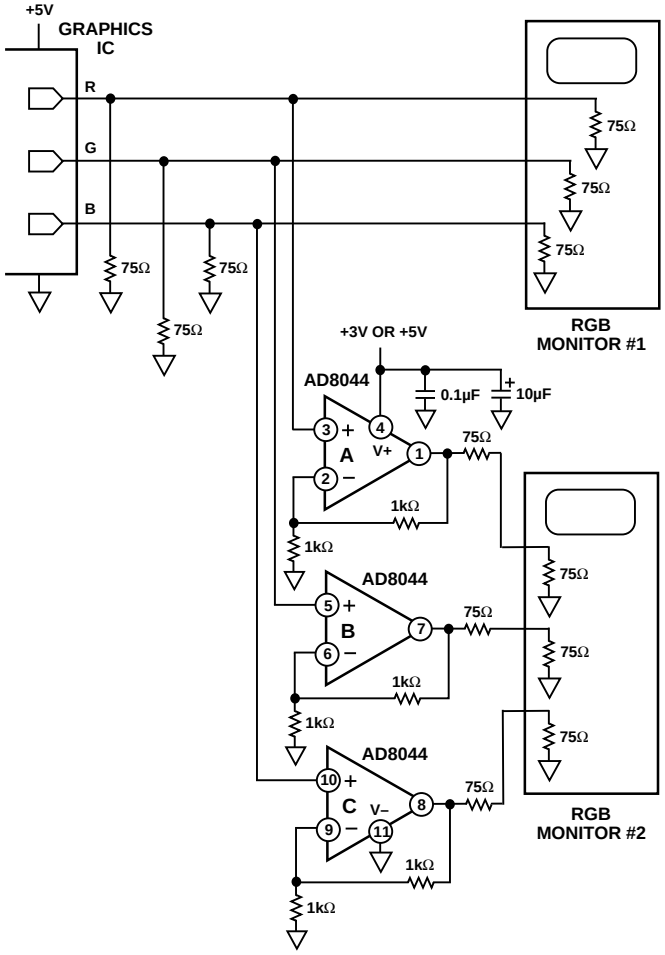


Figure 36. Single Supply RGB Video Driver

Figure 37 is an oscilloscope photo of the circuit in Figure 36 operating from a +3 V supply and driven by the Blue signal of a color bar pattern. Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700 mV peak. The output of the AD8044 is 1.4 V with the termination resistors providing a divide-by-two.

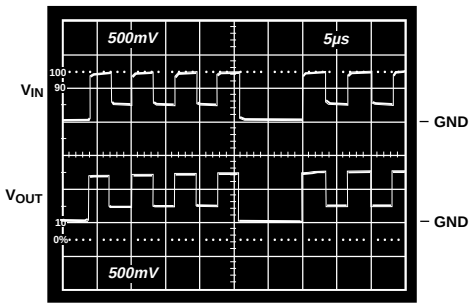


Figure 37. +3 V, RGB Buffer

HDSL Line Driver

HDSL or high-bit-rate digital subscriber line is becoming popular as a means to provide data communication at DS1 rates (1.544 MBPS) over moderate distances via conventional telephone twisted pair wires. In these systems, the transceiver at the customer's end is sometimes powered via the twisted pair from a power source at the central office. It is sometimes required to raise the dc voltage of the power source to compensate for IR drops in long lines or lines with narrow gauge wires.

Because of this, it is highly desirable to keep the power consumption of the customer's transceiver as low as possible. One means to realize significant power savings is to run the transceiver from a ±5 V supply instead of the more conventional ±12 V. This has not

The high output swing and current drive capability of the AD8042 make it ideally suited to this application. Figure 41 shows a circuit for the analog portion of an HDSL transceiver using the AD8042 as the line driver.

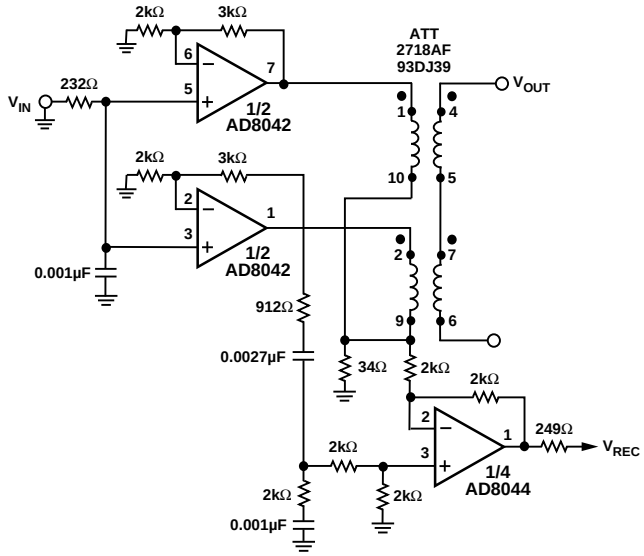


Figure 38. Twisted Pair Driver

Active Filters

Active filters at higher frequencies require wider bandwidth op amps to work effectively. Excessive phase shift produced by lower frequency op amps can significantly impact active filter performance.

Figure 39 shows an example of a 2 MHz biquad bandwidth filter that uses three op amps of an AD8044 package. Such circuits are sometimes used in medical ultrasound systems to lower the noise bandwidth of the analog signal before A/D conversion.

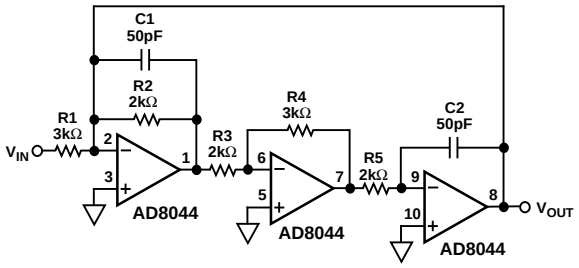


Figure 39. 2 MHz Biquad Bandpass Filter Using AD8044

The frequency response of the circuit is shown in Figure 40.

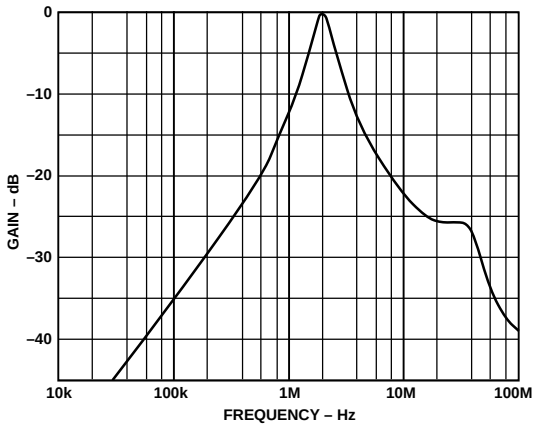


Figure 40. Frequency Response of 2 MHz Bandpass Biquad Filter

Layout Considerations

The specified high speed performance of the AD8044 requires careful attention to board layout and component selection. Proper RF design techniques and low-pass parasitic component selection are necessary.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed from the area near the input pins to reduce the stray capacitance.

Chip capacitors should be used for the supply bypassing. One end should be connected to the ground plane and the other within 1/8 inch of each power pin. An additional large (0.47 μF – 10 μF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily so close, to supply current for fast, large signal changes at the output.

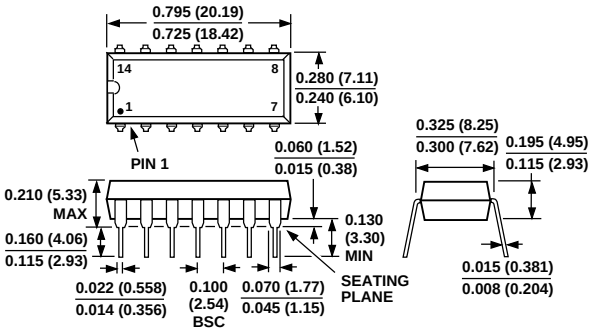
The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will significantly affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

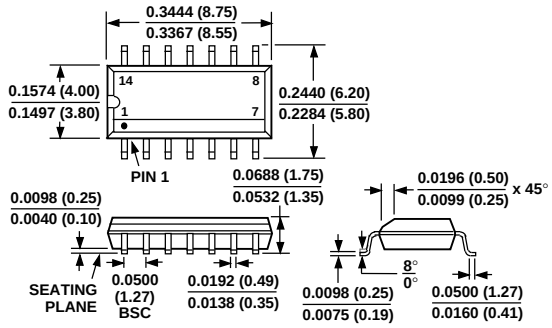
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead Plastic DIP
(N-14)



14-Lead SOIC
(R-14)



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National Semiconductor

January 1996

DS26C31T/DS26C31M CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (see Note 8). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

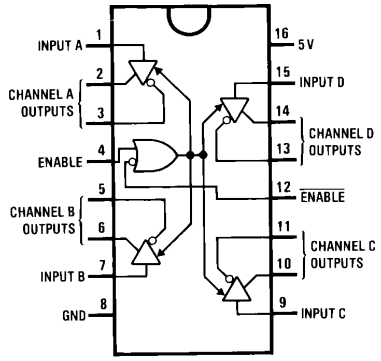
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs will not load line when V_{CC} = 0V
- DS26C31T meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount
- Mil-Std-883C compliant

Connection Diagrams

Dual-In-Line Package



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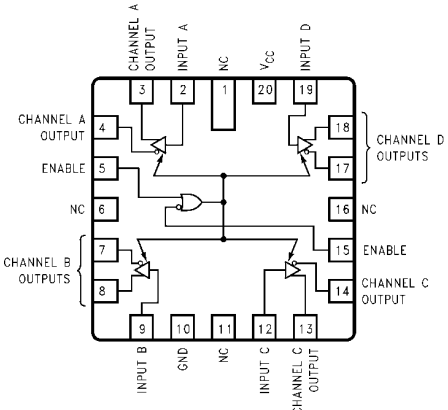
Top View

Order Number DS26C31TJ, DS26C31TM or DS26C31TN
See NS Package Number J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet

Order Number DS26C31ME/883, DS26C31MJ/883 or DS26C31MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier (E)



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

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FACT™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max. Power Dissipation (P_D) @25°C (Note 3)	
Ceramic "J" Pkg.	2419 mW
Plastic "N" Pkg.	1736 mW
SOIC "M" Pkg.	1226 mW
Ceramic "W" Pkg.	1182 mW
Ceramic "E" Pkg.	2134 mW
Lead Temperature (T_L) (Soldering, 4 sec.)	260°C

This device does not meet 2000V ESD Rating. (Note 13)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS26C31T	−40	+85	°C
DS26C31M	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 20 mA			0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100Ω (Note 5)		2.0	3.1		V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference In Differential Output	R_L = 100Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100Ω (Note 5)			1.8	3.0	V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$	Difference In Common Mode Output	R_L = 100Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current (Note 6)	DS26C31T I_{OUT} = 0 μA	V_{IN} = V_{CC} or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.0	mA
		DS26C31M I_{OUT} = 0 μA	V_{IN} = V_{CC} or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.1	mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}}$ = V_{IH}			±0.5	±5.0	μA

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SC}	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND (Notes 5, 7)		−30		−150	mA
I_{OFF}	Output Leakage Current Power Off (Note 5)	DS26C31T $V_{CC} = 0V$	$V_{OUT} = 6V$			100	μA
			$V_{OUT} = -0.25V$			−100	μA
		DS26C31M $V_{CC} = 0V$	$V_{OUT} = 6V$			100	μA
			$V_{OUT} = 0V$ (Note 8)			−100	μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N package at 13.89 mW/°C, J package 16.13 mW/°C, M package 9.80 mW/°C, E package 12.20 mW/°C, and W package 6.75 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Note 8: The DS26C31M (−55°C to +125°C) is tested with V_{OUT} between +6V and 0V while RS-422A condition is +6V and −0.25V.

Switching Characteristics $V_{CC} = 5V \pm 10\%$, $t_r \leq 6$ ns, $t_f \leq 6$ ns (*Figures 1, 2, 3* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	S1 Open	2	6	11	14	ns
Skew	(Note 9)	S1 Open		0.5	2.0	3.0	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
t_{PZH}	Output Enable Time	S1 Closed		11	19	22	ns
t_{PZL}	Output Enable Time	S1 Closed		13	21	28	ns
t_{PHZ}	Output Disable Time (Note 10)	S1 Closed		5	9	12	ns
t_{PLZ}	Output Disable Time (Note 10)	S1 Closed		7	11	14	ns
C_{PD}	Power Dissipation Capacitance (Note 11)			50			pF
C_{IN}	Input Capacitance			6			pF

Note 9: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 10: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 11: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

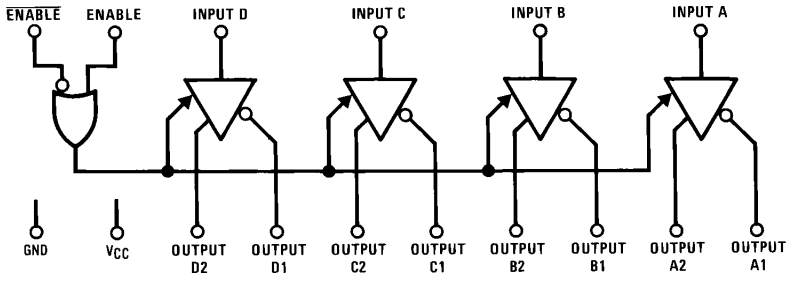
V_{CC} = 5V, T_A = 25°C, $t_r \leq 6$ ns, $t_f \leq 6$ ns (*Figures 2, 4, 5* and *6*) (Note 12)

Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	C_L = 30 pF S1 Closed S2 Closed	6	8	10	15	ns
Skew	(Note 9)	C_L = 30 pF S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times	C_L = 30 pF S1 Closed S2 Closed	4	6			ns
t_{PLZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Closed S2 Open	6	9	15	35	ns
t_{PHZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Open S2 Closed	4	7	15	25	ns
t_{PZL}	Output Enable Time	C_L = 30 pF S1 Closed S2 Open	14	20	20	30	ns
t_{PZH}	Output Enable Time	C_L = 30 pF S1 Open S2 Closed	11	17	20	30	ns

Note 12: This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or guaranteed.

Note 13: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥ 1500V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Logic Diagram



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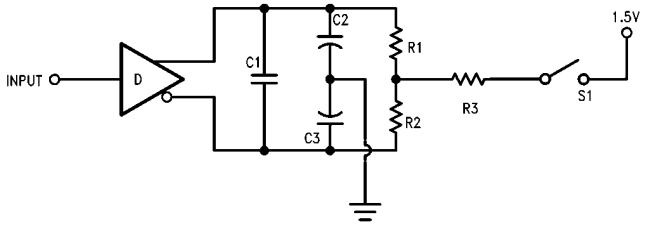
AC Test Circuit and Switching Time Waveforms



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Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

FIGURE 1. AC Test Circuit

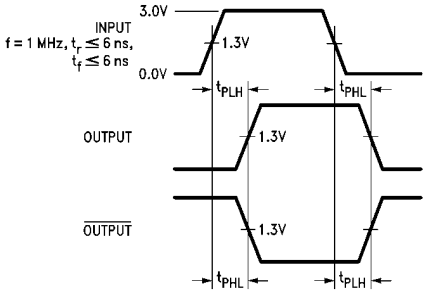

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FIGURE 2. Propagation Delays

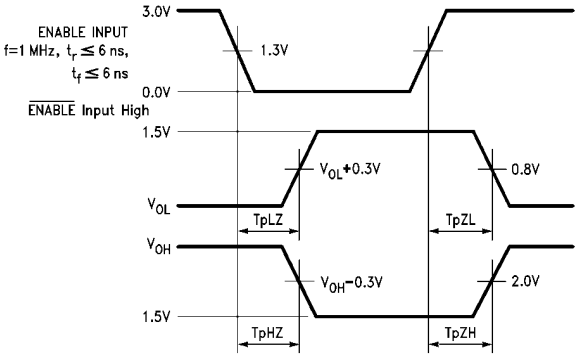

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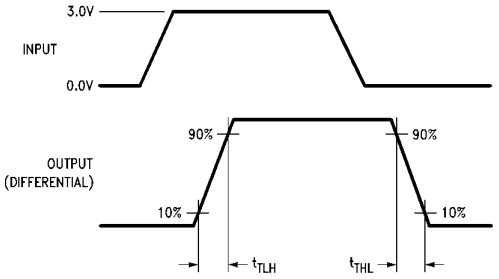
FIGURE 3. Enable and Disable Times



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Input pulse; f = 1 MHz, 50%; $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

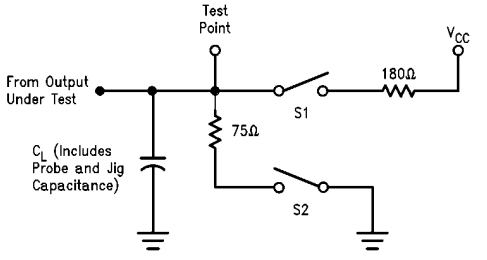

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FIGURE 5. Load AC Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)

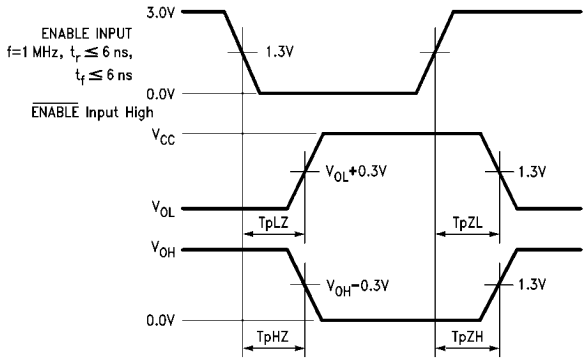

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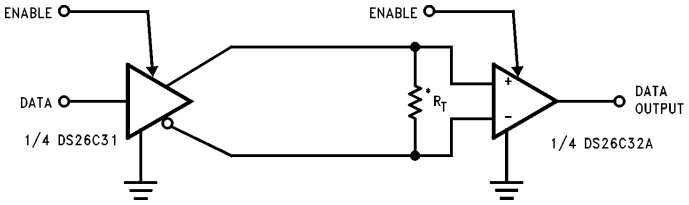
FIGURE 6. Enable and Disable Times for "LS-Type" Load

Typical Applications

Two-Wire Balanced System, RS-422



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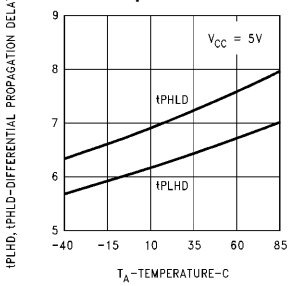
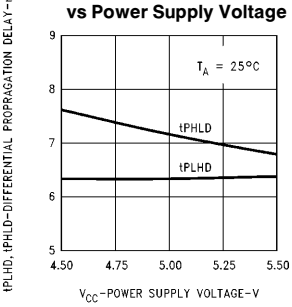
*R_T is optional although highly recommended to reduce reflection.

Typical Performance Characteristics

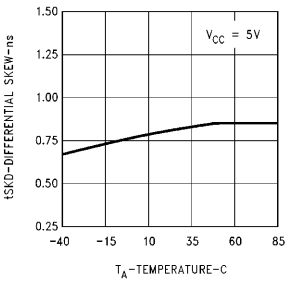
Differential Propagation Delay vs Temperature



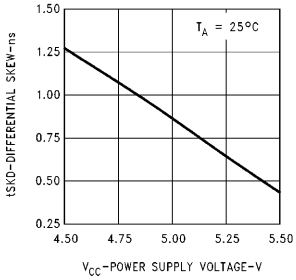
Differential Propagation Delay vs Power Supply Voltage



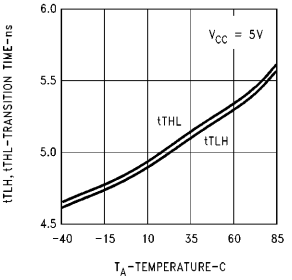
Differential Skew vs Temperature



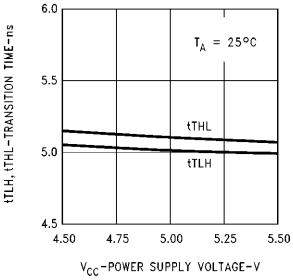
Differential Skew vs Power Supply Voltage



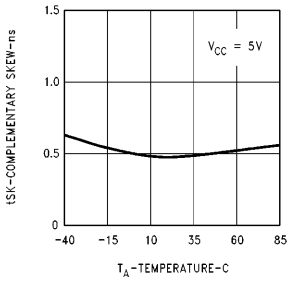
Differential Transition Time vs Temperature



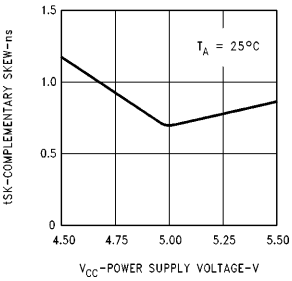
Differential Transition Time vs Power Supply Voltage



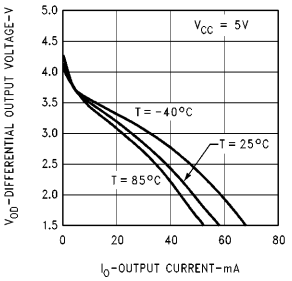
Complementary Skew vs Temperature



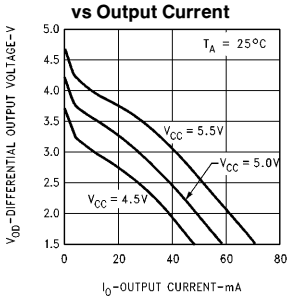
Complementary Skew vs Power Supply Voltage



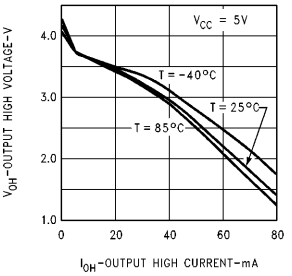
Differential Output Voltage vs Output Current



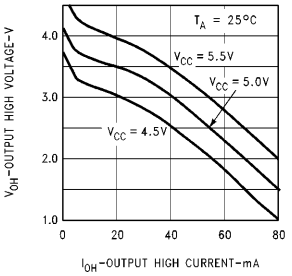
Differential Output Voltage vs Output Current



Output High Voltage vs Output High Current



Output High Voltage vs Output High Current



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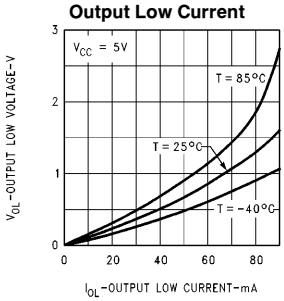
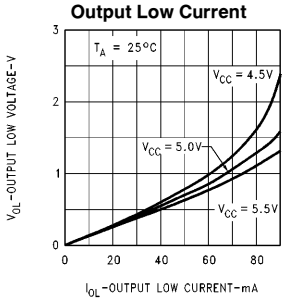
Typical Performance Characteristics (Continued)

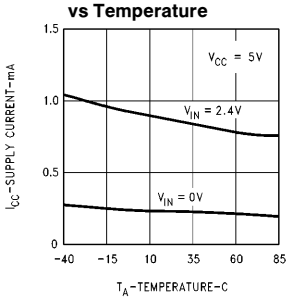
Output Low Voltage vs Output Low Current



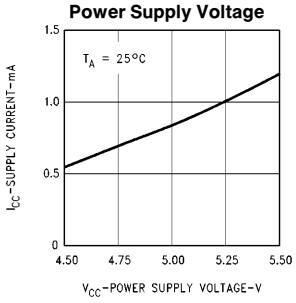
Output Low Voltage vs Output Low Current



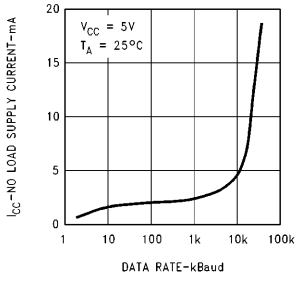
Supply Current vs Temperature



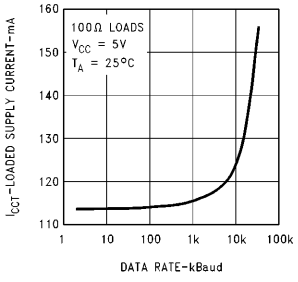
Supply Current vs Power Supply Voltage



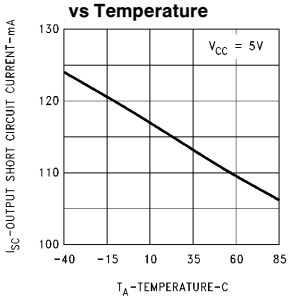
No Load Supply Current vs Data Rate



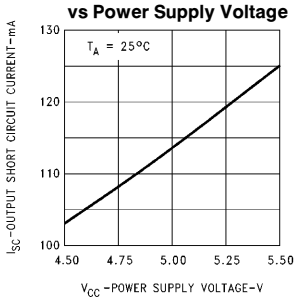
Loaded Supply Current vs Data Rate



Output Short Circuit Current vs Temperature



Output Short Circuit Current vs Power Supply Voltage



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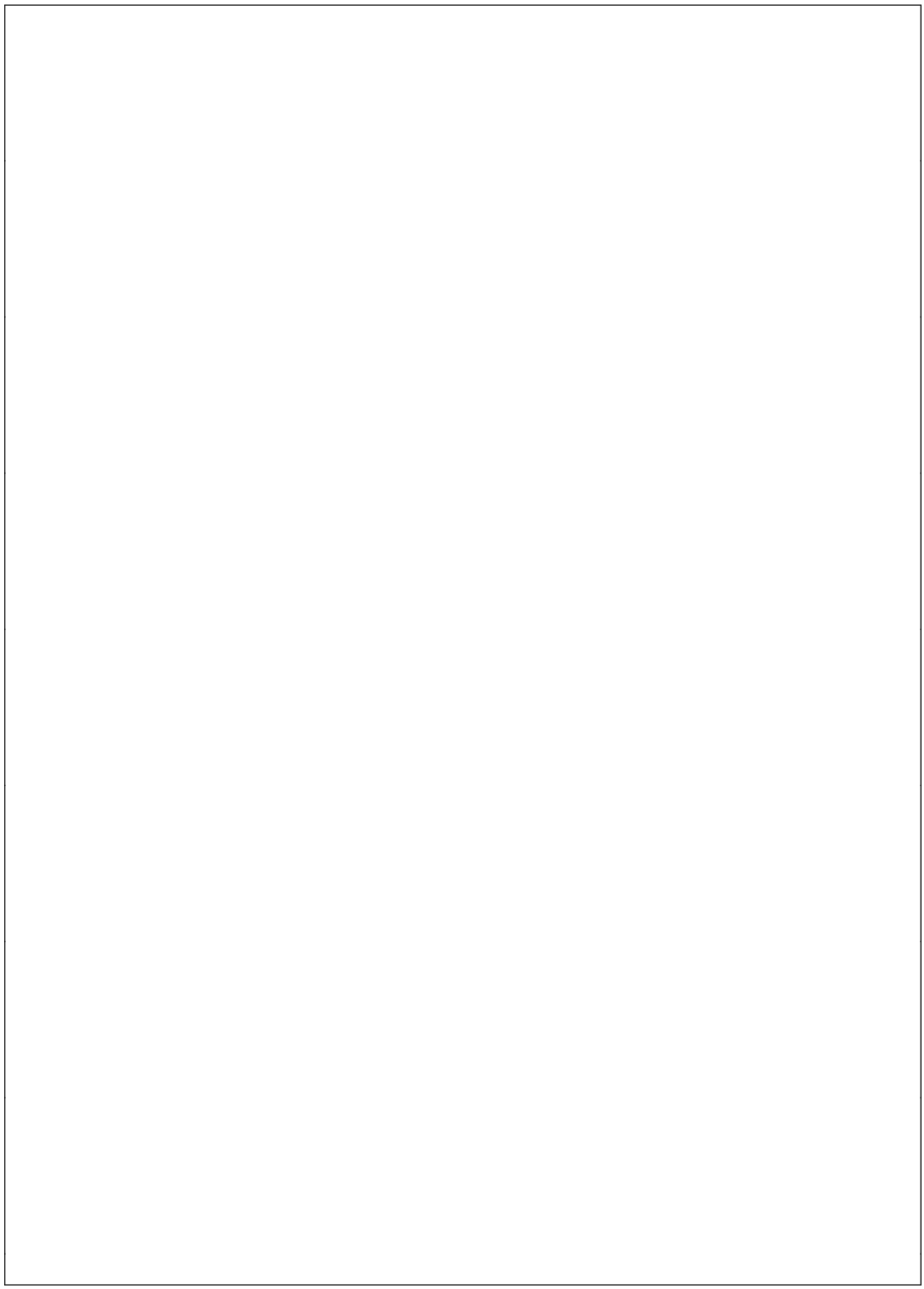
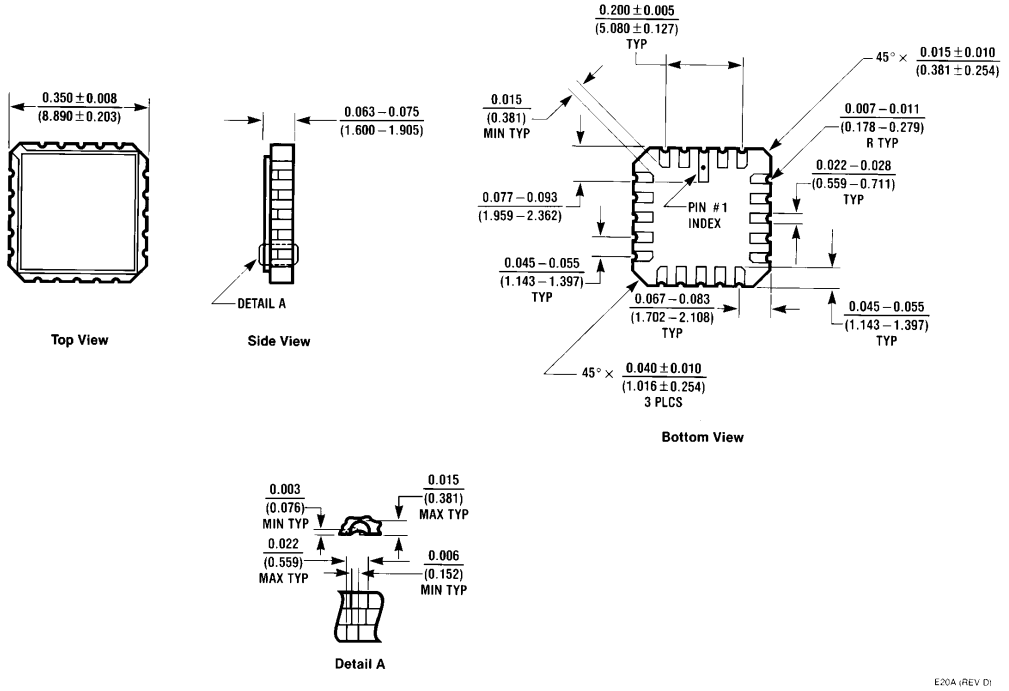
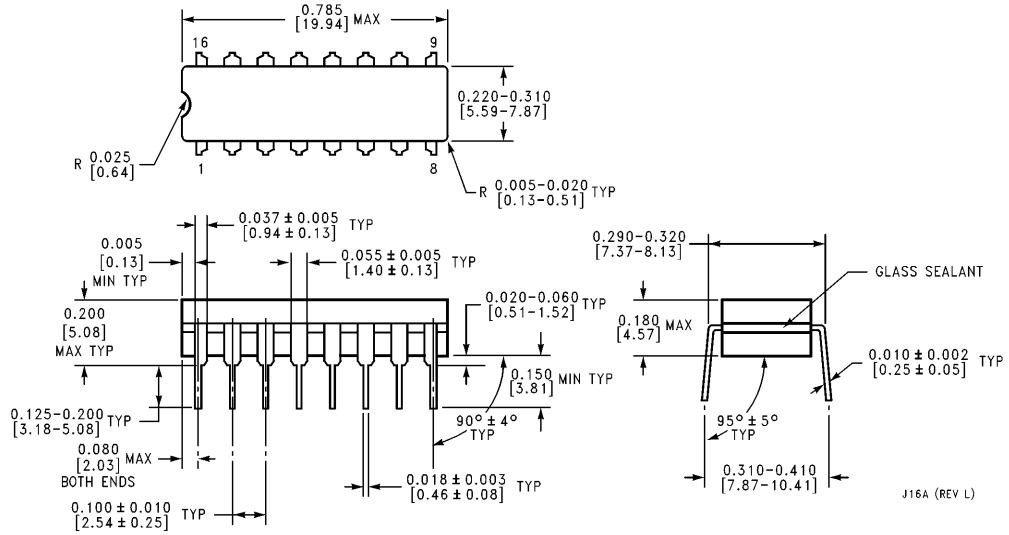


Physical Dimensions inches (millimeters)

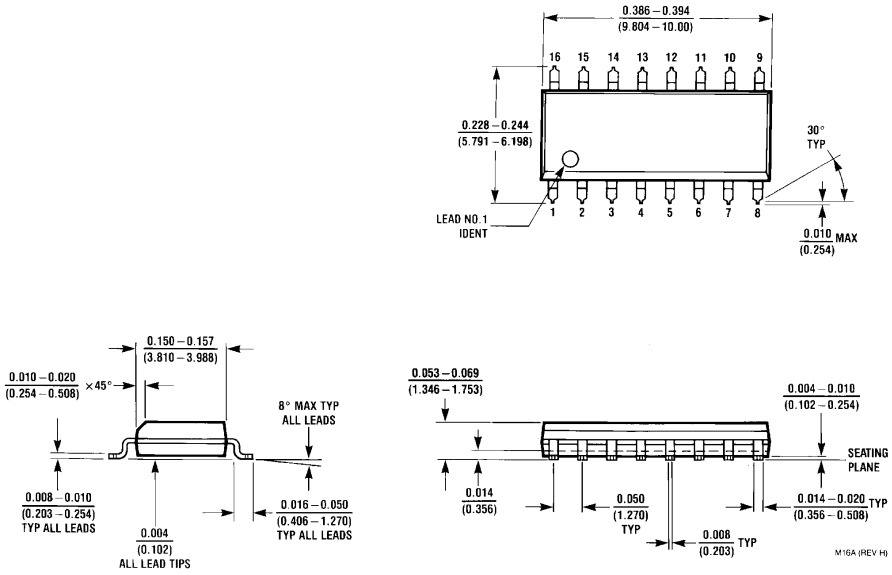


20-Lead Ceramic Leadless Chip Carrier (E)
Order Number DS26C31ME/883
NS Package Number E20A

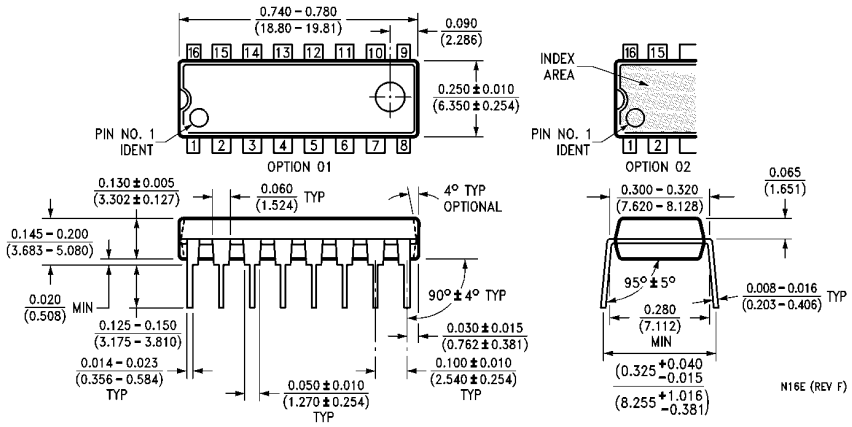


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DS26C31TJ or DS26C31MJ/883
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

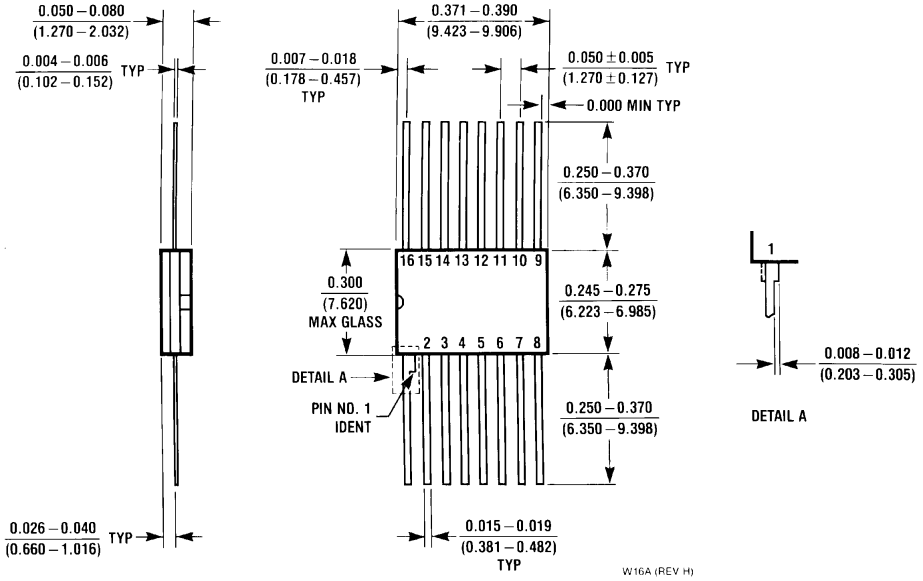


Molded Package Small Outline (M)
Order Number DS26C31TM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DS26C31TN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flatpak Package (W)
Order Number DS26C31MW/883
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

January 1996

DS26C32AT/DS26C32AM Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

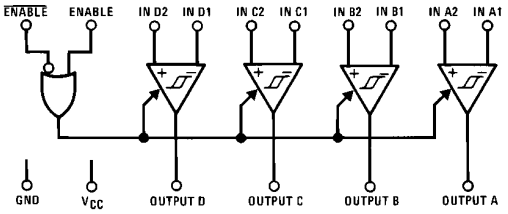
The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- CMOS design for low power
- ±0.2V sensitivity over input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses
- Available in Surface Mount
- Mil-Std-883C compliant

Logic Diagram



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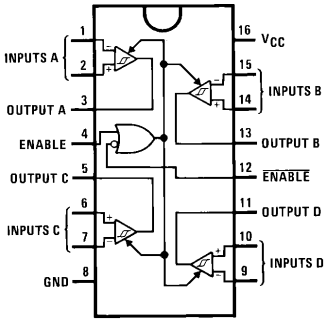
Connection Diagrams

Dual-In-Line Package



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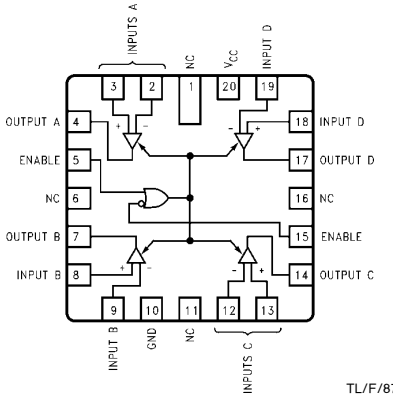
Top View

Order Number DS26C32ATJ, DS26C32ATM or DS26C32ATN
See NS Package J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet.

Order Number DS26C32AME/883, DS26C32AMJ/883 or DS26C32AMW/883
See NS Package E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH}$ (Max)	H
		$V_{ID} \leq V_{TH}$ (Min)	L
		Open	H

Z = TRI-STATE

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Pkg.	2308 mW
Plastic "N" Pkg.	1645 mW
SOIC "M" Pkg.	1190 mW
Ceramic "E" Pkg.	2108 mW
Ceramic "W" Pkg.	1215 mW
Maximum Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	−40	+85	°C
DS26C32AM	−55	+125	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$		−200	35	+200	mV
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	DS26C32AT	5.0	6.8	10	kΩ
			DS26C32AM	4.5	6.8	11	kΩ
I_{IN}	Input Current	$V_{IN} = +10V$, Other Input = GND	DS26C32AT		+1.1	+1.5	mA
			DS26C32AM		+1.1	+1.8	mA
		$V_{IN} = -10V$, Other Input = GND	DS26C32AT		−2.0	−2.5	mA
			DS26C32AM		−2.0	−2.7	mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, $V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA		3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, $V_{DIFF} = -1V$ I_{OUT} = 6.0 mA			0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage			2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage					0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{ENABLE} = V_{IL}$, $ENABLE = V_{IH}$			±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND				±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, $V_{DIF} = +1V$	DS26C32AT		16	23	mA
			DS26C32AM		16	25	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V			60		mV

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C32AT	DS26C32AM	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	$C_L = 50$ pF $V_{DIFF} = 2.5V$ $V_{CM} = 0V$	10	19	30	35	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	$C_L = 50$ pF $V_{DIFF} = 2.5V$ $V_{CM} = 0V$		4	9	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	22	29	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	$C_L = 50$ pF $R_L = 1000\Omega$ $V_{DIFF} = 2.5V$		13	23	29	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of ''Electrical Characteristics'' provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥2000V
All other pins ≥1000V
EIAJ (0Ω, 200 pF) ≥350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C, M Package 9.52 mW/°C, E Package 12.04 mW/°C, and W package 6.94 mW/°C.

Comparison Table of Switching Characteristics into ''LS-Type'' Load

(*Figures 4, 5,* and *6*) (Note 6)

Symbol	Parameter	Conditions	DS26C32A	DS26LS32A	Units
			Typ	Typ	
t_{PLH}	Input to Output	$C_L = 15$ pF	17	23	ns
t_{PHL}			19	23	ns
t_{LZ}	ENABLE to Output	$C_L = 5$ pF	13	15	ns
t_{HZ}			12	20	ns
t_{ZL}	ENABLE to Output	$C_L = 15$ pF	13	14	ns
t_{ZH}			13	15	ns

Note 6: This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested or guaranteed.

Test and Switching Waveforms

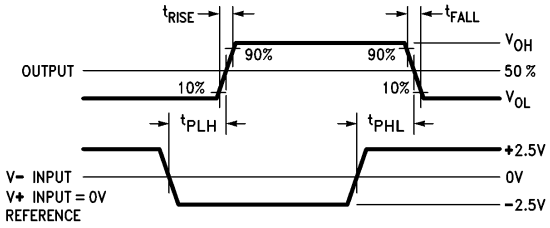

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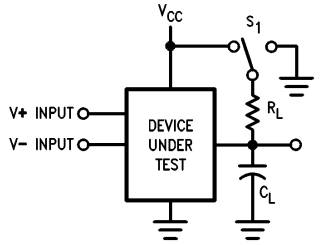
FIGURE 1. Propagation Delay



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C_L includes load and test jig capacitance.

$S_1 = V_{CC}$ for t_{PZL}, and t_{PLZ} measurements.

S_1 = Gnd for t_{PZH} and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

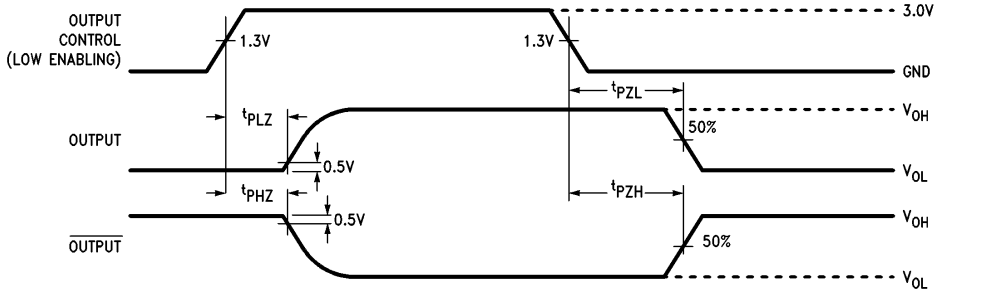

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FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuit and Switching Time Waveforms

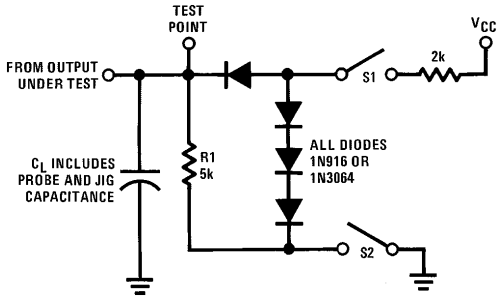

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FIGURE 4. Load Test Circuit for TRI-STATE Outputs for "LS-Type" Load

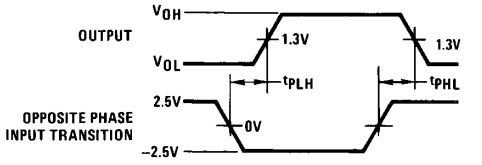

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FIGURE 5. Propagation Delay for "LS-Type" Load (Notes 7, 9)

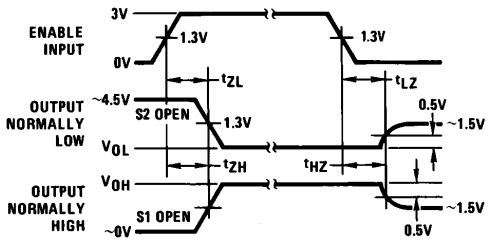

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FIGURE 6. Enable and Disable Times for "LS-Type" Load (Notes 8, 9)

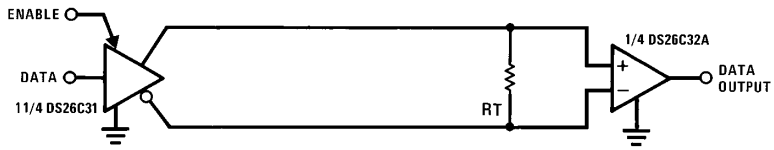
Note 7: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 8: S1 and S2 of load circuit are closed except where shown.

Note 9: Pulse generator for all pulses: Rate $\leq$ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced Systems, RS-422



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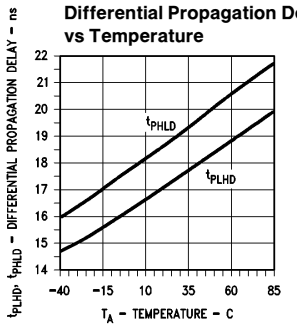
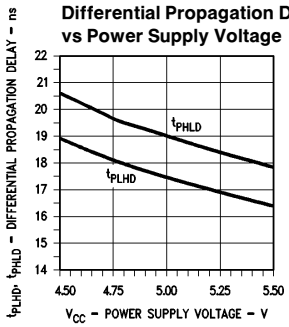
Typical Performance Characteristics

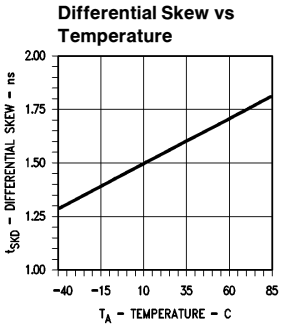
Differential Propagation Delay vs Temperature



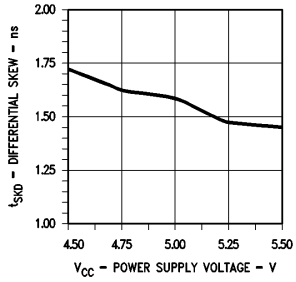
Differential Propagation Delay vs Power Supply Voltage



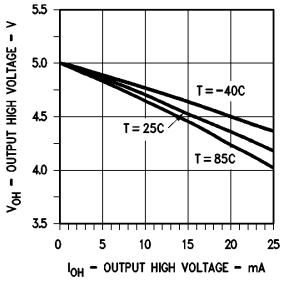
Differential Skew vs Temperature



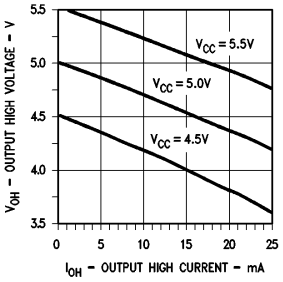
Differential Skew vs Power Supply Voltage



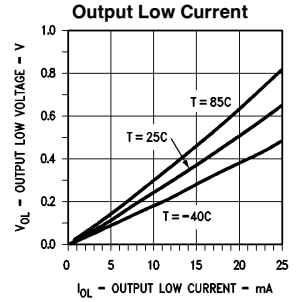
Output High Voltage vs Output High Current



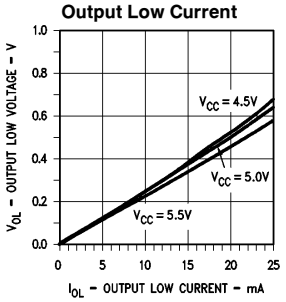
Output High Voltage vs Output High Current



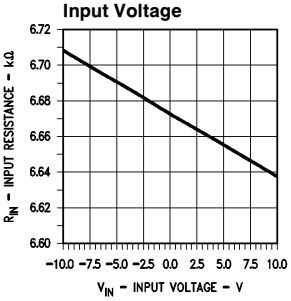
Output Low Voltage vs Output Low Current



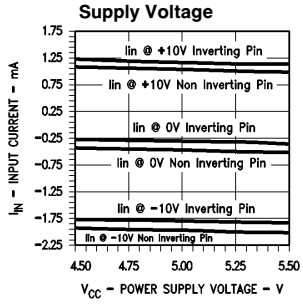
Output Low Voltage vs Output Low Current



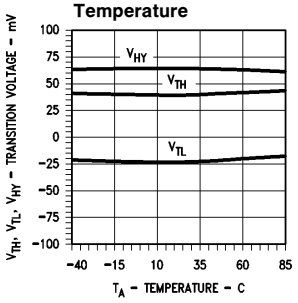
Input Resistance vs Input Voltage



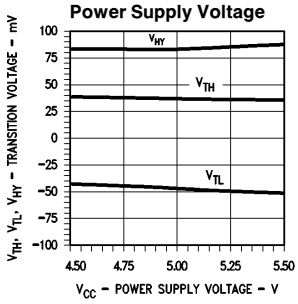
Input Current vs Power Supply Voltage



Hysteresis & Differential Transition Voltage vs Temperature



Hysteresis & Differential Transition Voltage vs Power Supply Voltage



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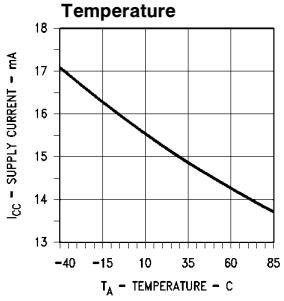
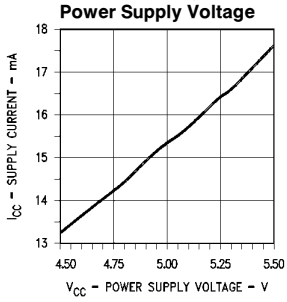
Typical Performance Characteristics (Continued)

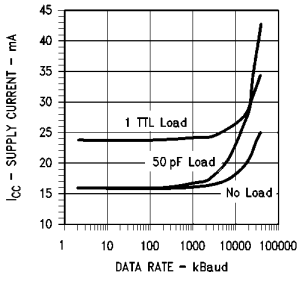
Supply Current vs Temperature



Disabled Supply Current vs Power Supply Voltage

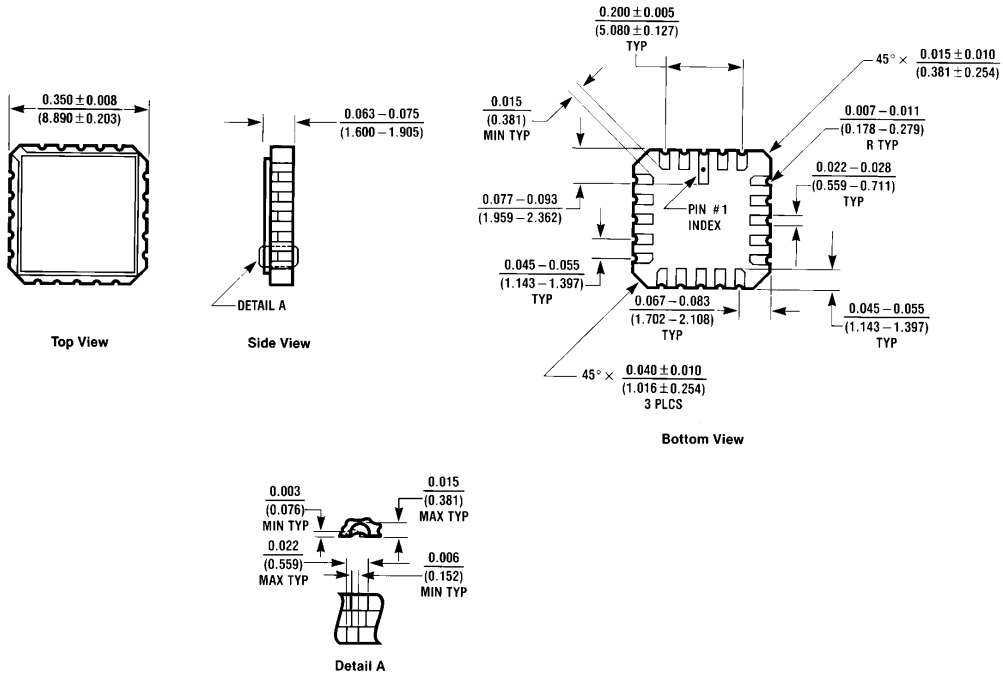


Supply Current vs Data Rate

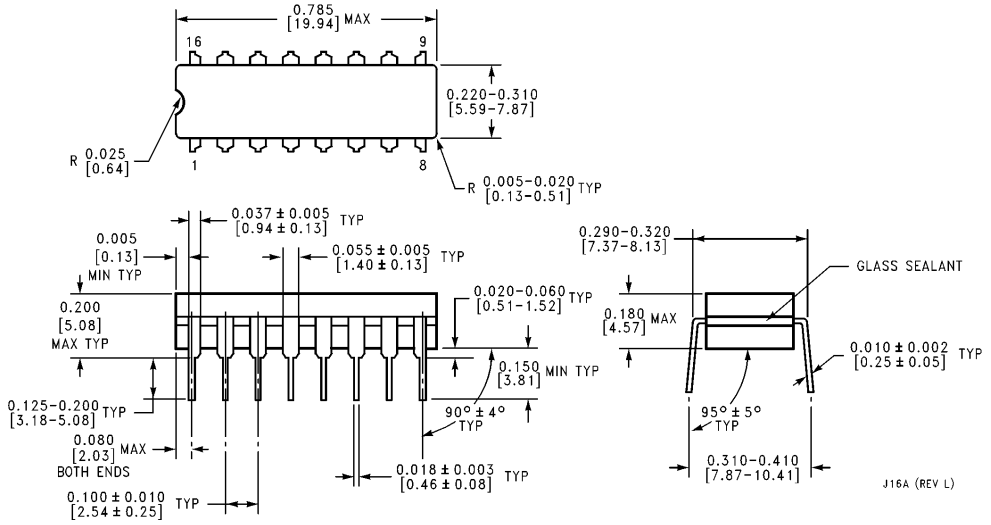


TL/F/8764–11

Physical Dimensions inches (millimeters)

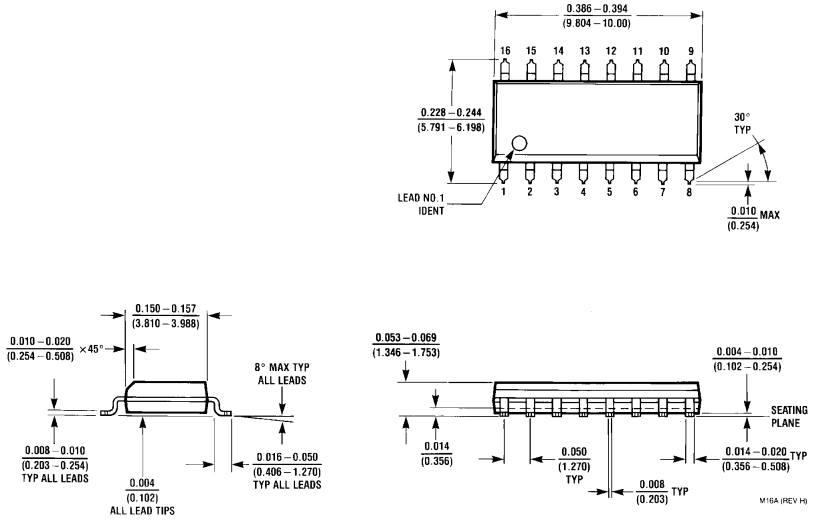


20-Lead Ceramic Leadless Chip Carrier (E)
Order Number DS26C32AME/883
NS Package Number E20A

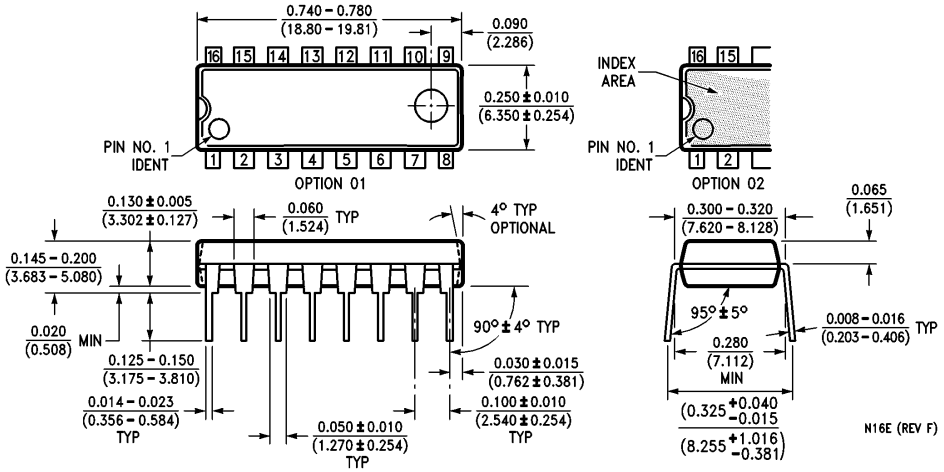


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DS26C32ATJ or DS26C32AMJ/883
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



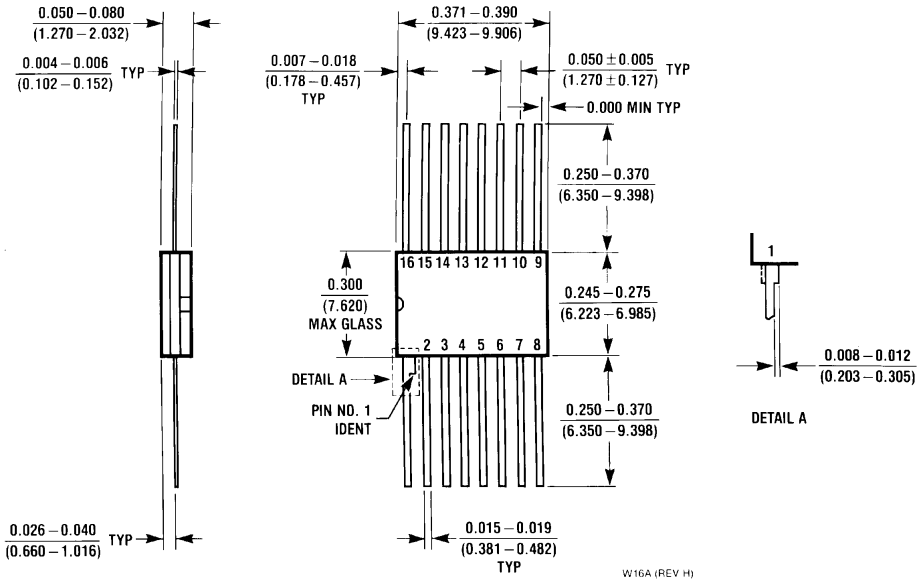
16-Lead Molded Small Outline Package (M)
Order Number DS26C32ATM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DS26C32ATN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)

Lit. # 103324



16-Lead Ceramic FlatPak (W)
Order Number DS26C32AMW/883
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Fax: (852) 2736-9960

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Tel: 81-043-299-2308
Fax: 81-043-299-2408

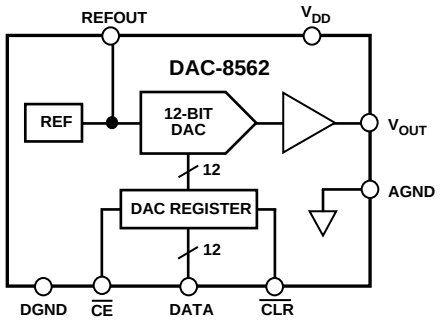
+5 Volt, Parallel Input Complete 12-Bit DAC

DAC8562

FEATURES
Complete 12-Bit DAC
No External Components
Single +5 Volt Operation
1 mV/Bit with 4.095 V Full Scale
True Voltage Output, ±5 mA Drive
Very Low Power –3 mW

APPLICATIONS
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC8562 is a complete, parallel input, 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DAC, is a rail-to-rail amplifier, latch and reference. The reference (REFOUT) is trimmed to 2.5 volts, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The DAC8562 is coded straight binary. The op amp output swings from 0 to +4.095 volts for a one millivolt per bit resolution, and is capable of driving ±5 mA. Built using low temperature-coefficient silicon-chrome thin-film resistors, excellent linearity error over temperature has been achieved as shown below in the linearity error versus digital input code plot.

Digital interface is parallel and high speed to interface to the fastest processors without wait states. The interface is very simple requiring only a single $\overline{CE}$ signal. An asynchronous $\overline{CLR}$ input sets the output to zero scale.

The DAC8562 is available in two different 20-pin packages, plastic DIP and SOL-20. Each part is fully specified for operation over –40°C to +85°C, and the full +5 V ± 5% power supply range.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8562/883 data sheet which specifies operation over the –55°C to +125°C temperature range.

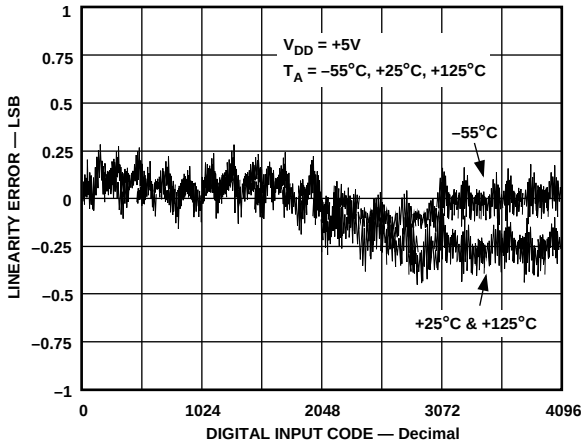


Figure 1. Linearity Error vs. Digital Input Code Plot

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

DAC8562–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 ± 5%, R_S = No Load, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 2	12			Bits
Relative Accuracy	INL	E Grade	–1/2	±1/4	+1/2	LSB
		F Grade	–1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data - FFF_H[3]				
		E Grade	4.087	4.095	4.103	V
		F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4		±16		ppm/°C
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H	±5	±7		mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[4]		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 5	5	7		mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA			0.1	%/mA
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 4			10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]						
Chip Enable Pulse Width	t_{CEW}		30			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Clear Pulse Width	t_{CLRW}		20			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough				35		nV sec
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB = 1 mV for 0 to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]Very little sink current is available at the REFOUT pin. Use external buffer if setting up a virtual ground.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{DD} = +5.0 V ± 5%, R_L = No Load, T_A = +25°C, applies to part number DAC8562GBC only, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Relative Accuracy	INL		–1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	–1	±3/4	+ 1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H	4.085	4.095	4.105	V
Reference Output Voltage	V_{REF}		2.490	2.500	2.510	V
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5 V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTE
[1]Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND and AGND ..... –0.3 V, +10 V
Logic Inputs to DGND .....–0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND .....–0.3 V, V_{DD} + 0.3 V
V_{REFOUT} to AGND .....–0.3 V, V_{DD} + 0.3 V
AGND to DGND ..... –0.3 V, V_{DD}
I_{OUT} Short Circuit to GND ..... 50 mA
Package Power Dissipation .....(T_J max – T_A)/θ_{JA}
Thermal Resistance θ_{JA}
20-Pin Plastic DIP Package (P) ..... 74°C/W
20-Lead SOIC Package (S) ..... 89°C/W
Maximum Junction Temperature (T_J max) ..... 150°C
Operating Temperature Range .....–40°C to +85°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

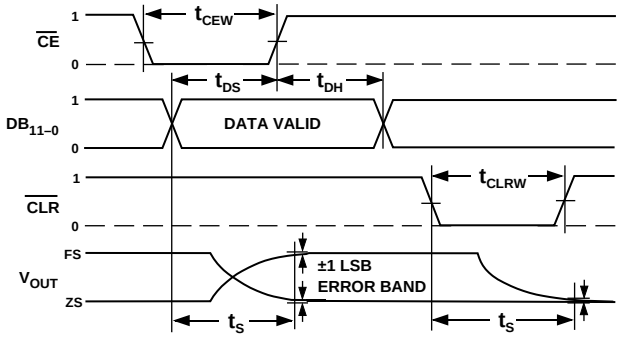


Figure 2. Timing Diagram

Table I. Control Logic Truth Table

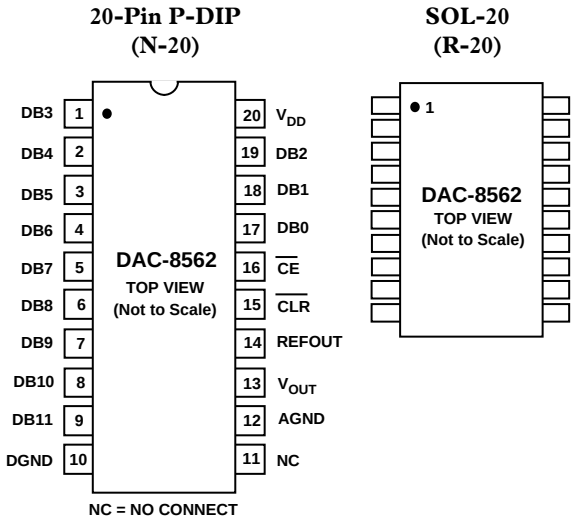
$\overline{CE}$	$\overline{CLR}$	DAC Register Function
H	H	Latched
L	H	Transparent
↑ +	H	Latched with New Data
X	L	Loaded with All Zeros
H	↑ +	Latched All Zeros

↑ + Positive Logic Transition; X Don't Care.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

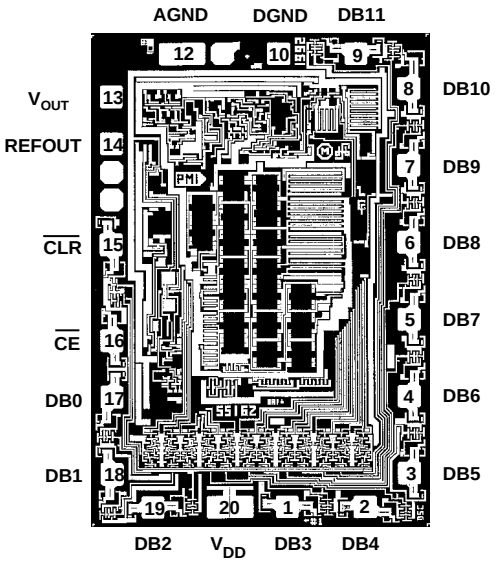
PIN CONFIGURATIONS



ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Option
DAC8562EP	±1/2	–40°C to +85°C	N-20
DAC8562FP	±1	–40°C to +85°C	N-20
DAC8562FS	±1	–40°C to +85°C	R-20
DAC8562GBC	±1	+25°C	Dice

DICE CHARACTERISTICS



SUBSTRATE IS COMMON WITH V_{DD}.

TRANSISTOR COUNT: 524

DIE SIZE: 0.70 X 0.105 INCH; 7350 SQ MILS

Table II. Nominal Output Voltage vs. Input Code

Binary	Hex	Decimal	Output (V)
0000 0000 0000	000	0	0.000 Zero Scale
0000 0000 0001	001	1	0.001
0000 0000 0010	002	2	0.002
0000 0000 1111	00F	15	0.015
0000 0001 0000	010	16	0.016
0000 1111 1111	0FF	255	0.255
0001 0000 0000	100	256	0.256
0001 1111 1111	1FF	511	0.511
0010 0000 0000	200	512	0.512
0011 1111 1111	3FF	1023	1.023
0100 0000 0000	400	1024	1.024
0111 1111 1111	7FF	2047	2.047
1000 0000 0000	800	2048	2.048 Half Scale
1100 0000 0000	C00	3072	3.072
1111 1111 1111	FFF	4095	4.095 Full Scale

PIN DESCRIPTIONS

Pin	Name	Description
20	V_{DD}	Positive supply. Nominal value +5 volts, ±5%.
1-9 17-19	DB0-DB11	Twelve Binary Data Bit inputs. DB11 is the MSB and DB0 is the LSB.
16	$\overline{CE}$	Chip Enable. Active low input.
15	$\overline{CLR}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale.
8	DGND	Digital ground for input logic.
12	AGND	Analog Ground. Ground reference for the internal bandgap reference voltage, the DAC, and the output buffer.
13	V_{OUT}	Voltage output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.
14	REFOUT	Nominal 2.5 V reference output voltage. This node must be buffered if required to drive external loads.
11	NC	No Connection. Leave pin floating.

OPERATION

The DAC8562 is a complete ready to use 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains a voltage-switched, 12-bit, laser-trimmed digital-to-analog converter, a curvature-corrected bandgap reference, a rail-to-rail output op amp, and a DAC register. The parallel data interface consists of 12 data bits, DB0–DB11, and a active low $\overline{CE}$ strobe. In addition, an asynchronous $\overline{CLR}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output (not available to the user) is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

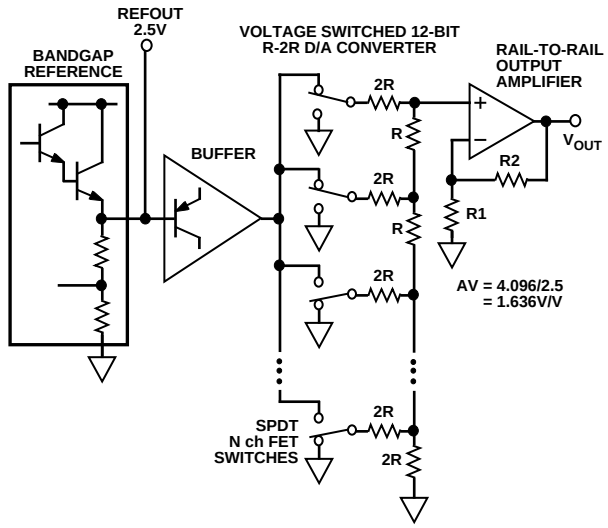


Figure 3. Equivalent DAC8562 Schematic of Analog Portion

The op amp has a 16 μs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the Typical Performances section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the –5% supply tolerance value of 4.75 volts.

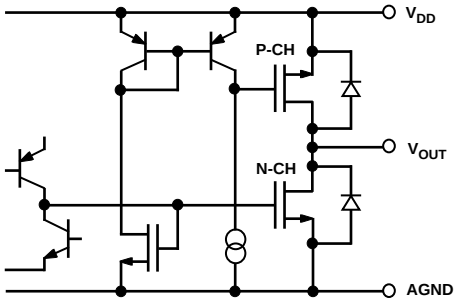


Figure 4. Equivalent Analog Output Circuit

Figures 5 and 6 in the typical performance characteristics section provide information on output swing performance near ground and full scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the REFOUT pin. Since REFOUT is not intended to drive external loads, it must be buffered–refer to the applications section for more information. The equivalent emitter follower output circuit of the REFOUT pin is shown in Figure 3.

Bypassing the REFOUT pin is not required for proper operation. Figure 7 shows broadband noise performance.

POWER SUPPLY

The very low power consumption of the DAC8562 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the DAC8562 is strongly dependent on the actual logic-input voltage-levels present on the DB0–DB11, $\overline{CE}$ and $\overline{CLR}$ pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total DAC8562 supply current as a function of the actual value of input logic voltage. Consequently for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the DB0–DB11 pins provides the lowest standby dissipation of 600 μA with a +5 V power supply.

As with any analog system, it is recommended that the DAC8562 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the DAC8562 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the DAC8562 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 11, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The DAC8562 has a 12-bit DAC register that simplifies interface to a 12-bit (or wider) data bus. The latch is controlled by the Chip Enable ($\overline{CE}$) input. If the application does not involve a data bus, wiring $\overline{CE}$ low allows direct operation of the DAC.

The data latch is level triggered and acquires data from the data bus during the time period when $\overline{CE}$ is low. When $\overline{CE}$ goes high, the data is latched into the register and held until $\overline{CE}$ returns low. The minimum time required for the data to be present on the bus before $\overline{CE}$ returns high is called the data setup time (t_{DS}) as seen in Figure 2. The data hold time (t_{DH}) is the amount of time that the data has to remain on the bus after $\overline{CE}$ goes high. The high speed timing offered by the DAC8562 provides for direct interface with no wait states in all but the fastest microprocessors.

Typical Performance Characteristics

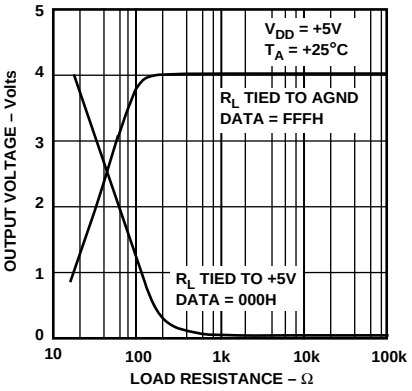


Figure 5. Output Swing vs. Load

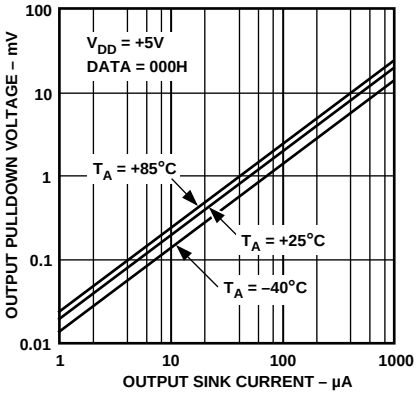


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

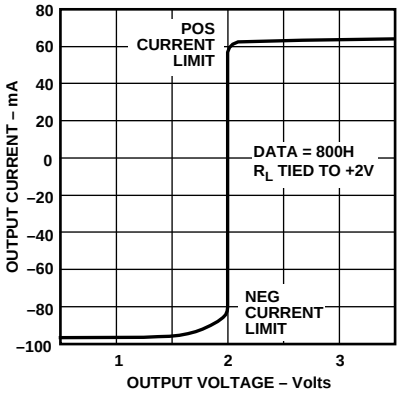


Figure 7. I_{OUT} vs. V_{OUT}

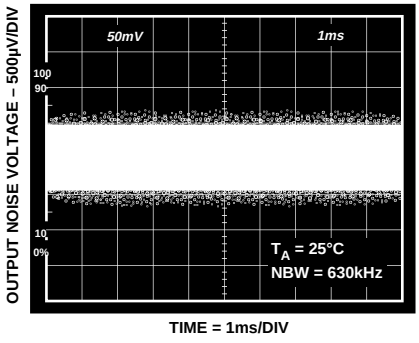


Figure 8. Broadband Noise

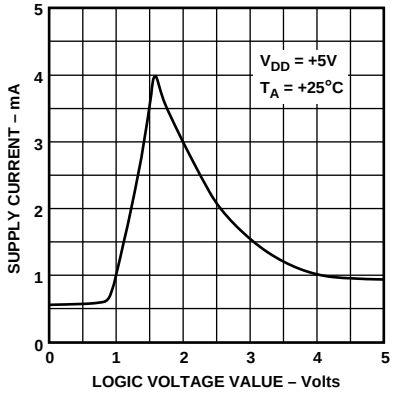


Figure 9. Supply Current vs. Logic Input Voltage

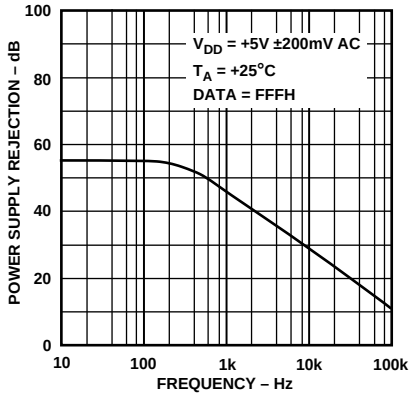


Figure 10. Power Supply Rejection vs. Frequency

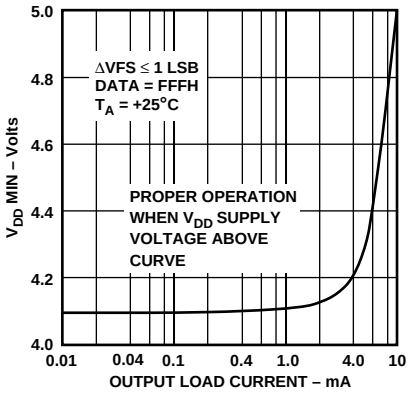


Figure 11. Minimum Supply Voltage vs. Load

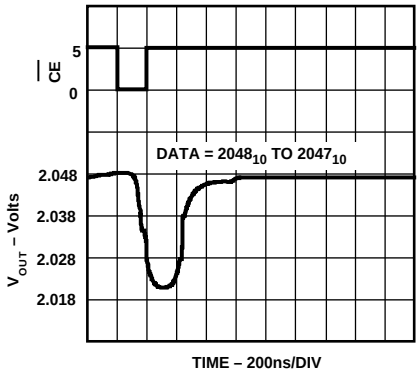


Figure 12. Midscale Transition Performance

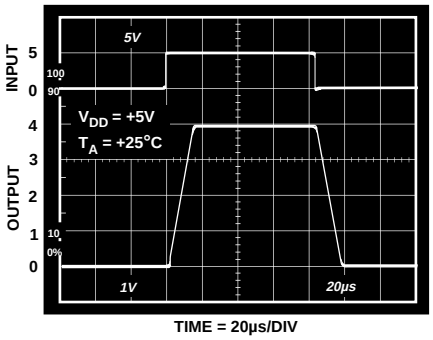


Figure 13. Large Signal Settling Time

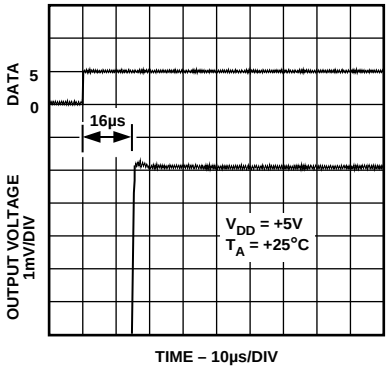


Figure 14. Output Voltage Rise Time Detail

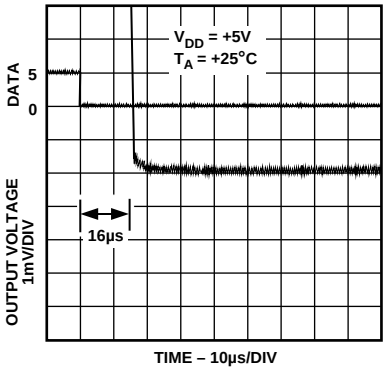


Figure 15. Output Voltage Fall Time Detail

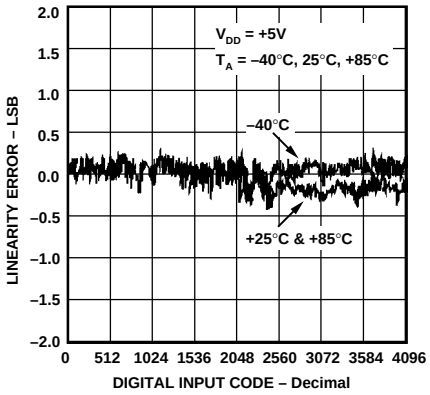


Figure 16. Linearity Error vs. Digital Code

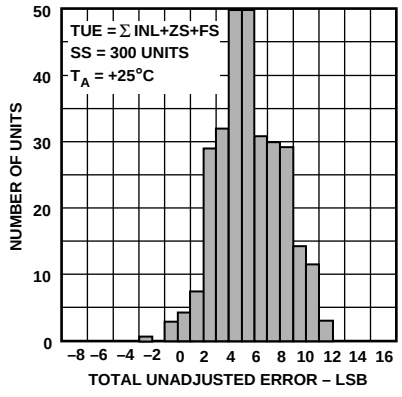


Figure 17. Total Unadjusted Error Histogram

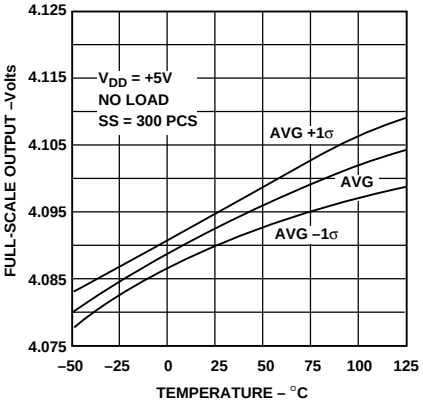


Figure 18. Full-Scale Voltage vs. Temperature

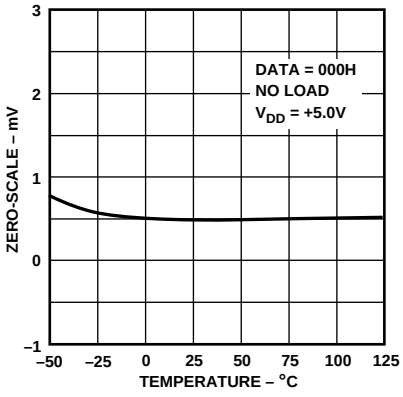


Figure 19. Zero-Scale Voltage vs. Temperature

DAC8562–Typical Performance Characteristics

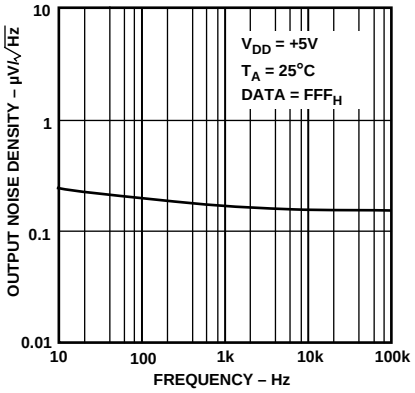


Figure 20. Output Voltage Noise Density vs. Frequency

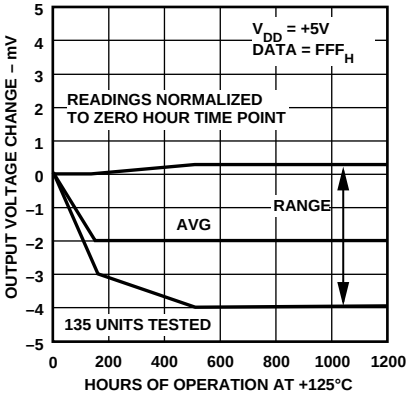


Figure 21. Long-Term Drift Accelerated by Burn-In

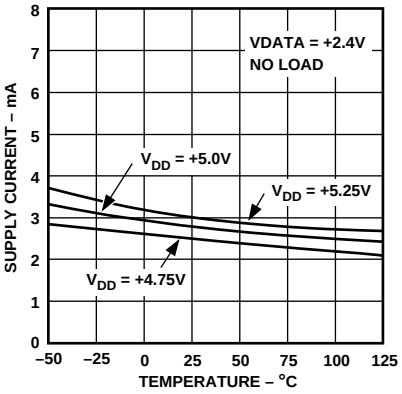


Figure 22. Supply Current vs. Temperature

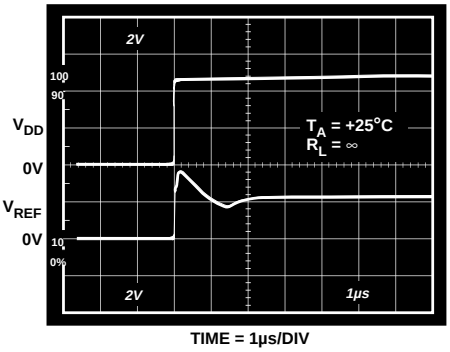


Figure 23. Reference Startup vs. Time

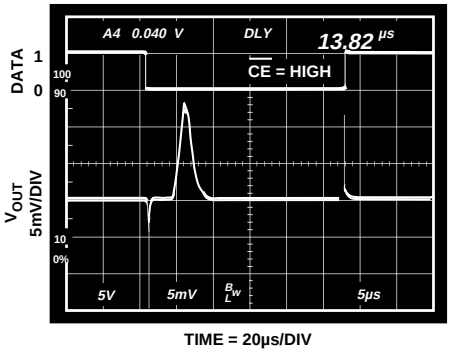


Figure 24. Digital Feedthrough vs. Time

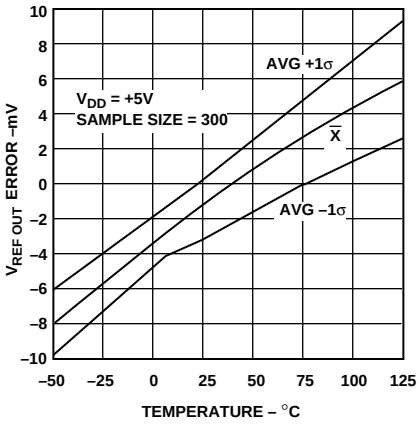


Figure 25. Reference Error vs. Temperature

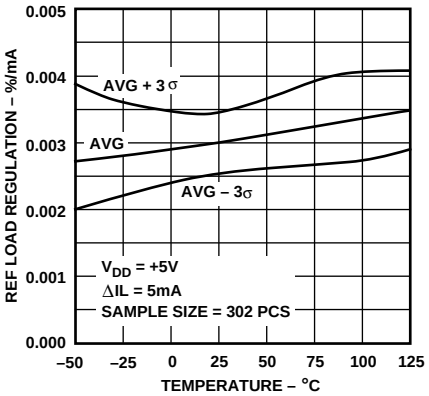


Figure 26. Reference Load Regulation vs. Temperature

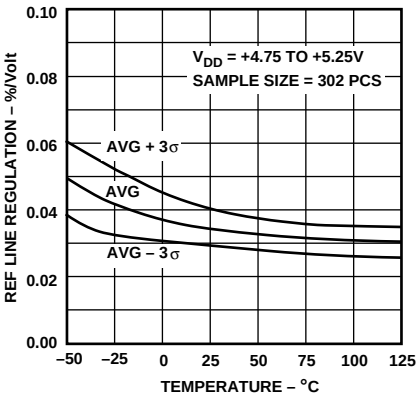


Figure 27. Reference Line Regulation vs. Temperature

APPLICATIONS SECTION

Power Supplies, Bypassing, and Grounding

All precision converter products require careful application of good grounding practices to maintain full-rated performance. Because the DAC8562 has been designed for +5 V applications, it is ideal for those applications under microprocessor or microcomputer control. In these applications, digital noise is prevalent; therefore, special care must be taken to assure that its inherent precision is maintained. This means that particularly good engineering judgment should be exercised when addressing the power supply, grounding, and bypassing issues using the DAC8562.

The power supply used for the DAC8562 should be well filtered and regulated. The device has been completely characterized for a +5 V supply with a tolerance of ±5%. Since a +5 V logic supply is almost universally available, it is not recommended to connect the DAC directly to an unfiltered logic supply without careful filtering. Because it is convenient, a designer might be inclined to tap a logic circuit s supply for the DAC's supply. Unfortunately, this is not wise because fast logic with nanosecond transition edges induces high current pulses. The high transient current pulses can generate glitches hundreds of millivolts in amplitude due to wiring resistances and inductances. This high frequency noise will corrupt the analog circuits internal to the DAC and cause errors. Even though their spike noise is lower in amplitude, directly tapping the output of a +5 V system supplies can cause errors because these supplies are of the switching regulator type that can and do generate a great deal of high frequency noise. Therefore, the DAC and any associated analog circuitry should be powered directly from the system power supply outputs using appropriate filtering. Figure 28 illustrates how a clean, analog-grade supply can be generated from a +5 V logic supply using a differential LC filter with separate power supply and return lines. With the values shown, this filter can easily handle 100 mA of load current without saturating the ferrite cores. Higher current capacity can be achieved with larger ferrite cores. For lowest noise, all electrolytic capacitors should be low ESR (Equivalent Series Resistance) type.

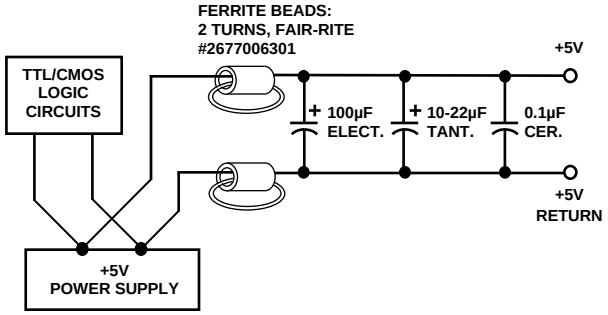


Figure 28. Properly Filtering a +5 V Logic Supply Can Yield a High Quality Analog Supply

The DAC8562 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (Pin 10) and AGND (Pin 12). The DGND pin is the return for the digital circuit sections of the DAC and serves as their input threshold reference point. Thus DGND should be connected to the same ground as the circuitry that drives the digital inputs.

Pin 12, AGND, serves as the supply rail for the internal voltage reference and the output amplifier. This pin should also serve as the reference point for all analog circuitry associated with the DAC8562. Therefore, to minimize any errors, it is recommended that the AGND connection of the DAC8562 be connected to a high quality analog ground. If the system contains any analog signal path carrying a significant amount of current, then that path should have its own return connection to Pin 12.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common to one place only. If the common tie point is remote and an accidental disconnection of that one common tie point were to occur due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the DAC8562, it is recommended that the common ground tie points be provided at each such device. If only one system ground can be connected directly to the DAC8562, it recommended that the analog common be used. If the system's AGND has suitably low impedance, then the digital signal currents flowing in it should not seriously affect the ground noise. The amount of digital noise introduced by connecting the two grounds together at the device will not adversely affect system performance due to loss of digital noise immunity.

Generous bypassing of the DAC's supply goes a long way in reducing supply line-induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic is recommended. The decoupling capacitors should be connected between the DAC's supply pin (Pin 20) and the analog ground (Pin 12). Figure 29 shows how the DGND, AGND, and bypass connections should be made to the DAC8562.

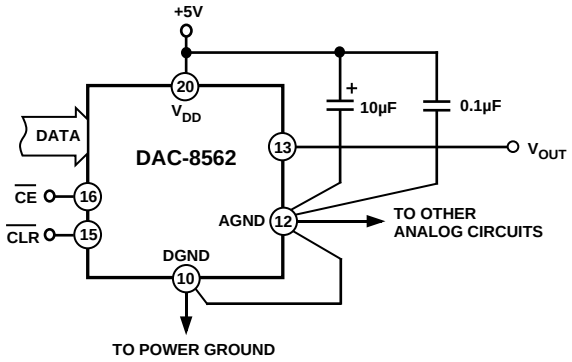


Figure 29. Recommended Grounding and Bypassing Scheme for the DAC-8562

Unipolar Output Operation

This is the basic mode of operation for the DAC8562. As shown in Figure 30, the DAC8562 has been designed to drive loads as low as 820 Ω in parallel with 500 pF. The code table for this operation is shown in Table III.

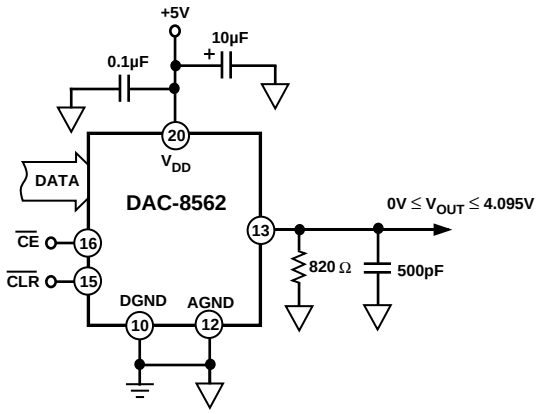


Figure 30. Unipolar Output Operation

Table III. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

Operating the DAC8562 on +12 V or +15 V Supplies Only

Although the DAC8562 has been specified to operate on a single, +5 V supply, a single +5 V supply may not be available in many applications. Since the DAC8562 consumes no more than 6 mA, maximum, then an integrated voltage reference, such as the REF02, can be used as the DAC8562 +5 V supply. The configuration of the circuit is shown in Figure 31. Notice that the reference's output voltage requires no trimming because of the REF02's excellent load regulation and tight initial output voltage tolerance. Although the maximum supply current of the DAC8562 is 6 mA, local bypassing of the REF02's output with at least 0. 1 µF at the DAC's voltage supply pin is recommended to prevent the DAC's internal digital circuits from affecting the DAC's internal voltage reference.

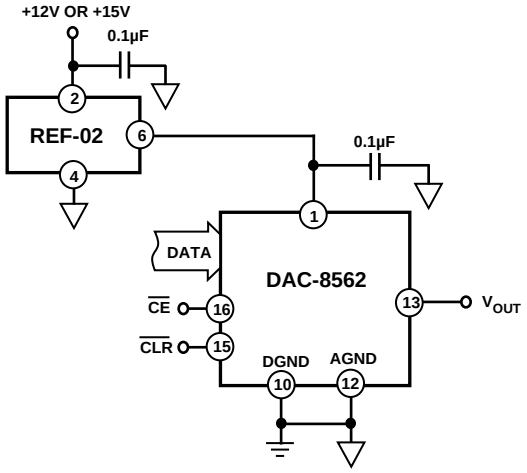


Figure 31. Operating the DAC8562 on +12 V or +15 V Supplies Using a REF02 Voltage Reference

Measuring Offset Error

One of the most commonly specified endpoint errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volt. There are some DACs where offset errors may be present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the DAC8562, for example, the zero-scale error is specified to be +3 LSBs. Since zero scale coincides with zero volt, it is not possible to measure negative offset error.

By adding a pull-down resistor from the output of the DAC8562 to a negative supply as shown in Figure 32, offset errors can now be read at zero code. This configuration forces the output P-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 µA maximum.

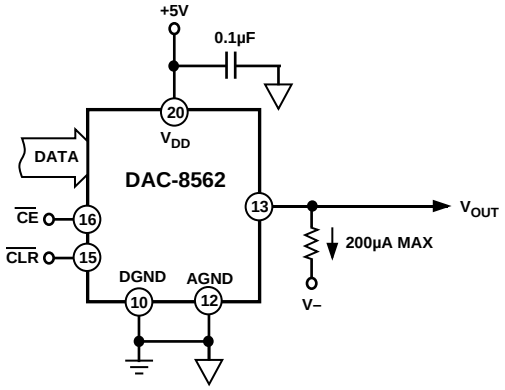


Figure 32. Measuring Zero-Scale or Offset Error

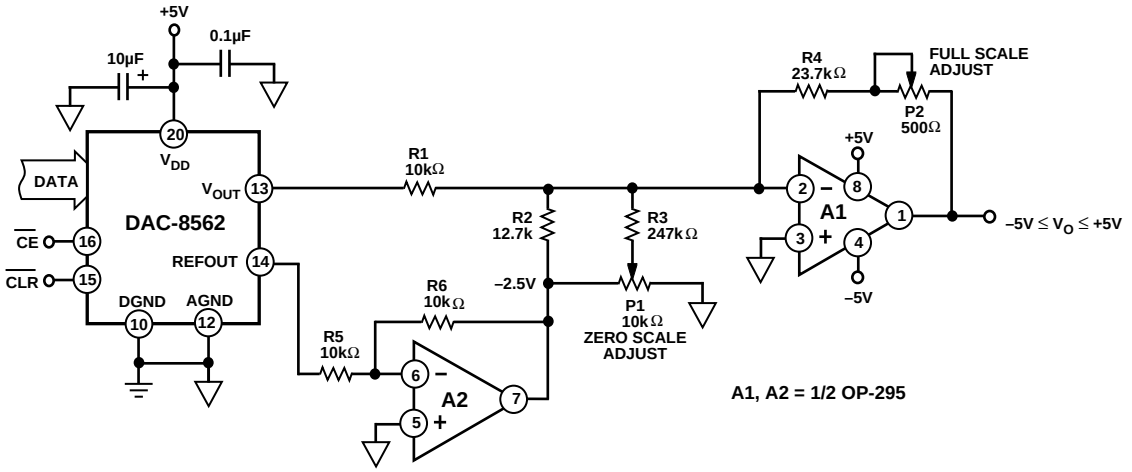


Figure 33. Bipolar Output Operation

Bipolar Output Operation

Although the DAC8562 has been designed for single supply operation, bipolar operation is achievable using the circuit illustrated in Figure 33. The circuit uses a single supply, rail-to-rail OP295 op amp and the DAC's internal +2.5 V reference to generate the –2.5 V reference required to level-shift the DAC output voltage. The circuit has been configured to provide an output voltage in the range –5 V ≤ V_{OUT} ≤ +5 V and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table IV provides the relationship between the digital codes and output voltage.

The transfer function of the circuit is given by:

$$V_O = -1\,mV \times Digital\ Code \times \left(\frac{R4}{R1}\right) + 2.5 \times \left(\frac{R4}{R2}\right)$$

and, for the circuit values shown, becomes:

$$V_O = -2.44\ mV \times Digital\ Code + 5\,V$$

Table IV. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	–4 9976
801	2049	–2.44E–3
800	2048	0
7FF	2047	+2.44E–3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, R4, R5, and R6 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors while an R4 to R1 and R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 34 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim The output voltage is coded in offset binary and is given by:

$$V_O = 1\,mV \times Digital\ Code \times \left(\frac{R4}{R3+R4}\right) \times \left(1 + \frac{R2}{R1}\right)$$

$$-REFOUT \times \left(\frac{R2}{R1}\right)$$

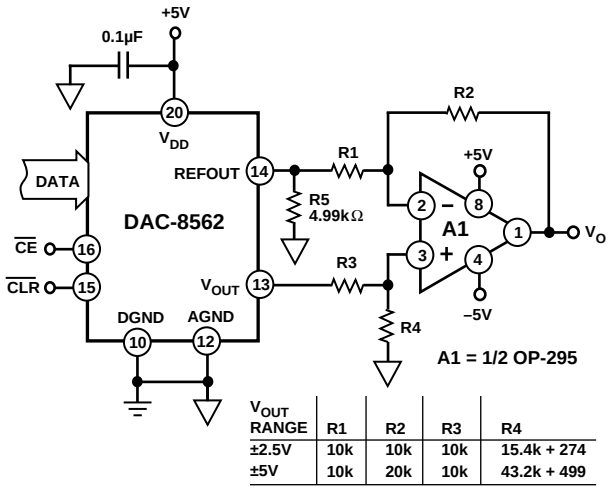
For the ±2 5 V output range and the circuit values shown in the table, the transfer equation becomes:

$$V_O = 1.22\,mV \times Digital\ Code - 2.5\,V$$

Similarly, for the ±5 V output range, the transfer equation becomes:

$$V_O = 2.44\,mV \times Digital\ Code - 5\,V$$

Note that, for ±5 V output voltage operation, R5 is required as a pull-down for REFOUT. Or, REFOUT can be buffered by an op amp configured as a follower that can source and sink current.



V_{OUT} RANGE	R1	R2	R3	R4
±2.5V	10k	10k	10k	15.4k + 274
±5V	10k	20k	10k	43.2k + 499

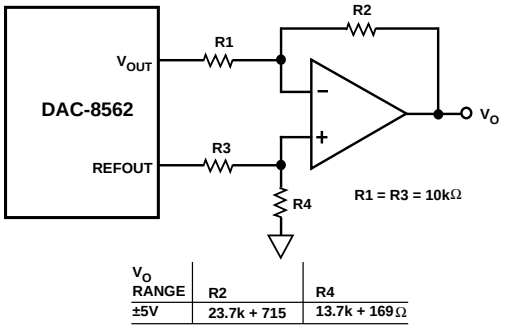
Figure 34. Bipolar Output Operation Without Trim Version 1

Alternatively, the output voltage can be coded in complementary offset binary using the circuit in Figure 35. This configuration eliminates the need for a pull-down resistor or an op amp for REFOUT The transfer equation of the circuit is given by:

$$V_O = -1\,mV \times Digital\ Code \times \left(\frac{R2}{R1}\right) + REFOUT \times \left(\frac{R4}{R3+R4}\right) \times \left(1+\frac{R2}{R1}\right)$$

and, for the values shown, becomes:

$$V_O = -2.44\,mV \times Digital\ Code + 5\,V$$



V_O RANGE	R2	R4
±5V	23.7k + 715	13.7k + 169Ω

Figure 35 Bipolar Output Operation Without Trim Version 2

Generating a Negative Supply Voltage

Some applications may require bipolar output configuration, but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, only +12 V, +15 V, and/or +5 V are available. Shown in Figure 36 is a method of generating a negative supply voltage using one CD4049, a CMOS hex inverter, operating on +12 V or +15 V. The circuit is essentially a charge pump where two of the six are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2. The remaining four inverters are wired in parallel for higher output current. The square-wave output is level translated by C2 to a negative-going signal, rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump will provide an output voltage of –5 V for current loading in the range 0.5 mA ≤ I_{OUT} ≤ 10 mA with a +15 V supply and 0.5 mA ≤ I_{OUT} ≤ 7 mA with a +12 V supply.

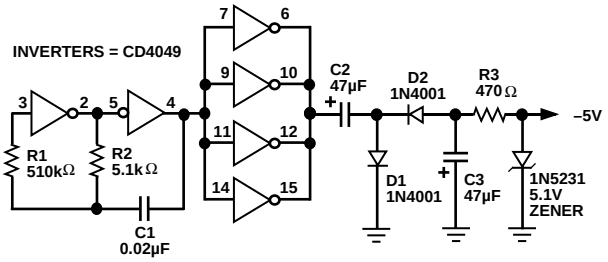


Figure 36. Generating a –5 V Supply When Only +12 V or +15 V Are Available

Audio Volume Control

The DAC8562 is well suited to control digitally the gain or attenuation of a voltage controlled amplifiers. In professional audio mixing consoles, music synthesizers, and other audio processors, VCAs, such as the SSM2018, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of the audio level when the slew rate of the analog input control voltage, V_C, is properly chosen. The circuit in Figure 37 illustrates a volume control application using the DAC8562 to control the attenuation of the SSM2018.

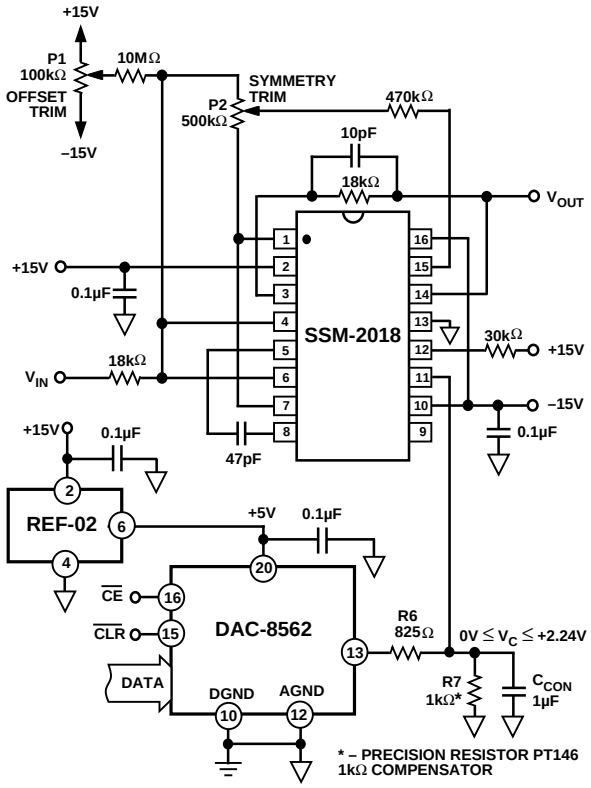


Figure 37. Audio Volume Control

Since the supply voltage available in these systems is typically ±15 V or ±18 V, a REF02 is used to supply the +5 V required to power the DAC. No trimming of the reference is required because of the reference's tight initial tolerance and low supply current consumption of the DAC8562. The SSM2018 is configured as a unity-gain buffer when its control voltage equals 0 volt. This corresponds to a 000_H code from the DAC8562. Since the SSM2018 exhibits a gain constant of –28 mV/dB (typical), the DAC's full-scale output voltage has to be scaled down by R6 and R7 to provide 80 dB of attenuation when the digital code equals FFF_H. Therefore, every DAC LSB corresponds to 0.02 dB of attenuation. Table V illustrates the attenuation versus digital code of the volume control circuit.

Table V. SSM2018 VCA Attenuation vs. DAC8562 Input Code

Hexadecimal Number in DAC Register	Control Voltage (V)	VCA Attenuation (dB)
000	0	0
400	+0.56	20
800	+1.12	40
C00	+1.68	60
FFF	+2.24	80

To compensate for the SSM2018's gain constant temperature coefficient of –3300 ppm/°C, a 1 kΩ, temperature-sensitive resistor (R7) manufactured by the Precision Resistor Company with a temperature coefficient of +3500 ppm/°C is used. A C_{CON} of 1 µF provides a control transition time of 1 ms which yields a click-free change in the audio channel attenuation. Symmetry and offset trimming details of the VCA can be found in the SSM2018 data sheet.

Information regarding the PT146 1 kΩ "Compensator" can be obtained by contacting:

Precision Resistor Company, Incorporated
10601 75th Street North
Largo, FL 34647
(813) 541-5771

A High-Compliance, Digitally Controlled Precision Current Source

The circuit in Figure 38 shows the DAC8562 controlling a high-compliance, precision current source using an AMP05 instrumentation amplifier. The AMP05's reference pin becomes the input, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS}. Voltage gain is set to unity, so the transfer function is given by the following equation:

$$I_{OUT} = \frac{V_{IN}}{R_{CS}}$$

If R_{CS} equals 100 Ω, the output current is limited to +10 mA with a 1 V input. Therefore, each DAC LSB corresponds to 2.4 µA. If a bipolar output current is required, then the circuit in Figure 33 can be modified to drive the AMP05's reference pin with a ±1 V input signal.

Potentiometer P1 trims the output current to zero with the input at 0 V. Fine gain adjustment can be accomplished by adjusting R1 or R2.

A Digitally Programmable Window Detector

A digitally programmable, upper/lower limit detector using two DAC8562s is shown in Figure 39. The required upper and lower limits for the test are loaded into each DAC individually by controlling HDAC/$\overline{\text{LDAC}}$. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero which will turn the red LED on.

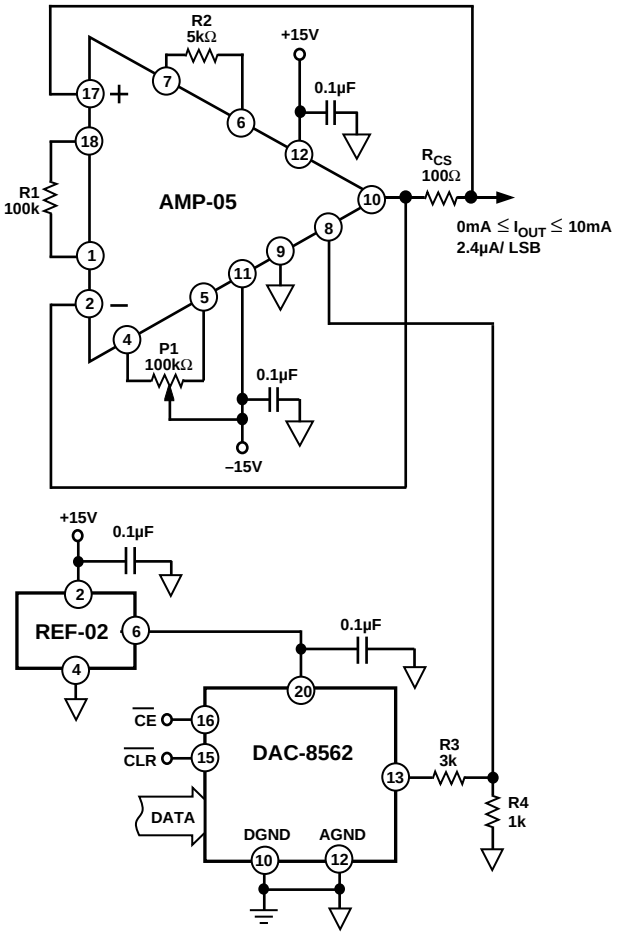


Figure 38. A High-Compliance, Digitally Controlled Precision Current Source

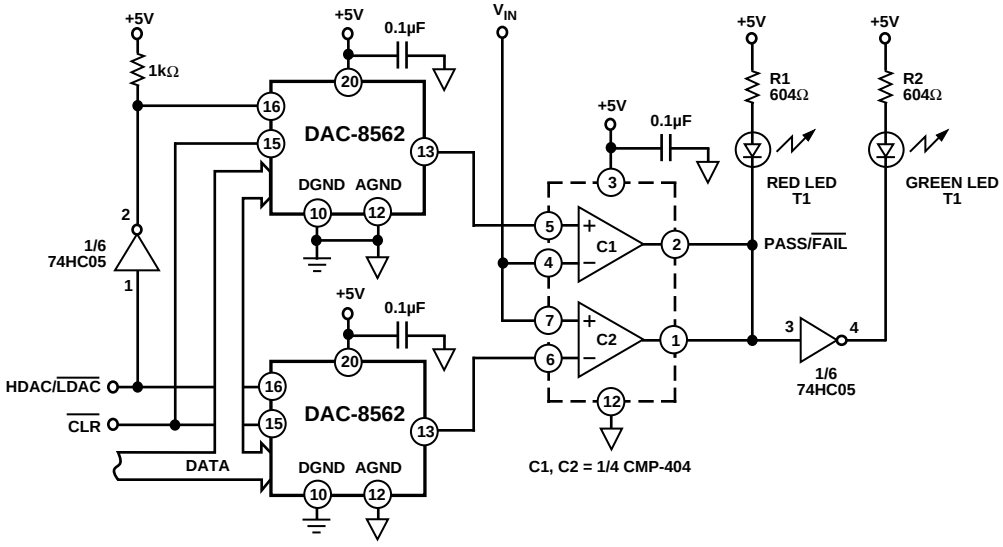


Figure 39. A Digitally Programmable Window Detector

Decoding Multiple DAC8562s

The $\overline{CE}$ function of the DAC8562 can be used in applications to decode a number of DACs. In this application, all DACs receive the same input data; however, only one of the DACs' $\overline{CE}$ input is asserted to transfer its parallel input register contents into the DAC. In this circuit, shown in Figure 40, the $\overline{CE}$ timing is generated by a 74HC139 decoder and should follow the DAC8562's standard timing requirements. To prevent timing errors, the 74HC139 should not be activated by its $\overline{ENABLE}$ input while the coded address inputs are changing. A simple timing circuit, R1 and C1, connected to the DACs' $\overline{CLR}$ pins resets all DAC outputs to zero during power-up.

MICROPROCESSOR INTERFACING

DAC-8562–MC68HC11 INTERFACE

The circuit illustrated in Figure 41 shows a parallel interface between the DAC8562 and a popular 8-bit microcontroller, the M68HC11, which is configured in a single-chip operating mode. The interface circuit consists of a pair of 74ACT11373 transparent latches and an inverter. The data is loaded into the latches in two 8-bit bytes; the first byte contains the four most significant bits, and the lower 8 bits are in the second byte. Data is taken from the microcontroller's port B output lines, and three interface control lines, $\overline{CLR}$, $\overline{CE}$, and MSB/$\overline{LSB}$, are controlled by the M68HC11's PC2, PC1, and PC0 output lines, respectively. To transfer data into the DAC, PC0 is set, enabling U1's outputs. The first data byte is loaded into U1 where the four least significant bits of the byte are connected to MSB–DB8. PC0 is then cleared; this latches U1's inputs and enables U2's outputs. U2s outputs now become DB7–DB0. The DAC output is updated with the contents of U1 and U2 when PC1 is cleared. The DAC's $\overline{CLR}$ input, controlled by the M68HC11's PC2 output line, provides an asynchronous clear function that sets the DAC's output to zero. Included in this section is the source code for operating the DAC-8562–M68HC11 interface.

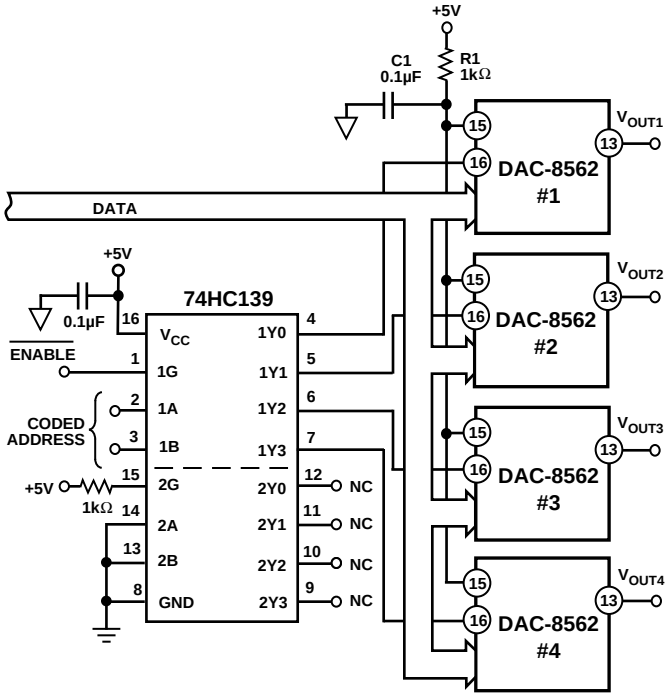


Figure 40. Decoding Multiple DAC8562s Using the $\overline{CE}$ Pin

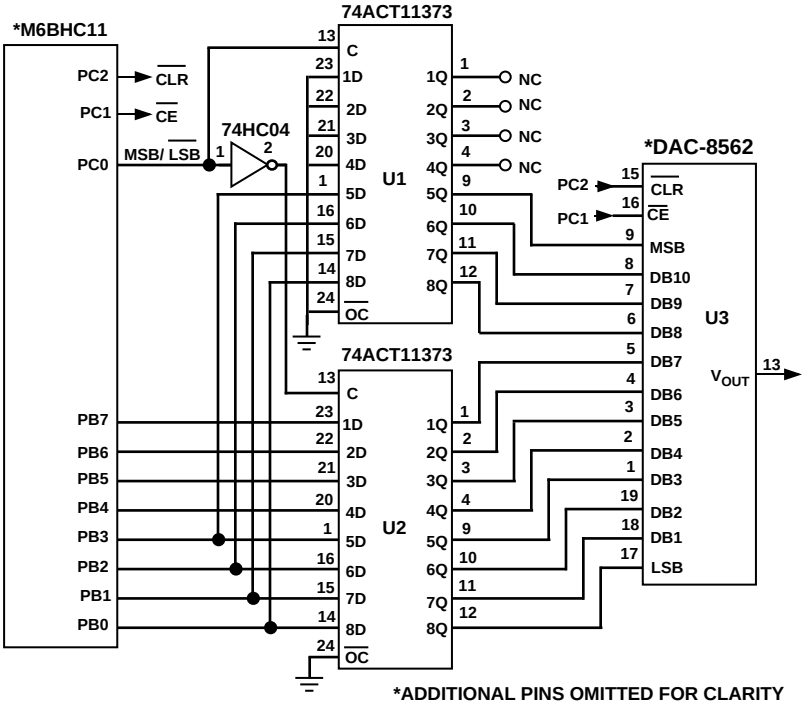


Figure 41. DAC8562 to MC68HC11 Interface

DAC8562 – M68HC11 Interface Program Source Code

```
*
* DAC8562 to M68HC11 Interface Assembly Program
* Adolfo A. Garcia
* September 14, 1992
*
* M68HC11 Register definitions
*
PORTB   EQU   $1004
PORTC   EQU   $1003          Port C control register
*                            "0,0,0,0;0,CLR/,CE/,MSB-LSB/"
DDRC    EQU   $1007          Port C data direction
*
* RAM variables:             MSBS are encoded from 0 (Hex) to F (Hex)
*                            LSBS are encoded from 00 (Hex) to F (Hex)
*                            DAC requires two 8-bit loads
*
MSBS    EQU   $00            Hi-byte: "0,0,0,0;MSB,DB10,DB9,DB8"
LSBS    EQU   $01            Lo-byte: "DB7,DB6,DB5,DB4;DB3,DB2,
                             DB1,DB0"
*
* Main Program
*
        ORG   $C000          Start of user's RAM in EVB
INIT    LDS   #$CFFF         Top of C page RAM
*
* Initialize Port C Outputs
*
        LDAA  #$07           0,0,0,0;0,1,1,1
        STAA  DDRC           CLR/,CE/, and MSB-LSB/ are now enabled
                             as outputs
        LDAA  #$06           0,0.0,0;0,1,1,0
*                            CLR/-Hi, CE/-Hi, MSB-LSB/-Lo
        STAA  PORTC          Initialize Port C Outputs
*
* Call update subroutine
*
        BSR   UPDATE         Xfer 2 8-bit words to DAC8562
        JMP   $E000          Restart BUFFALO
*
* Subroutine UPDATE
*
UPDATE  PSHX                 Save registers X, Y, and A
        PSHY
        PSHA
*
* Enter contents of the Hi-byte input register
*
        LDAA  #$0A           0,0,0,0;1,0,1,0
        STAA  MSBS           MSBS are set to 0A (Hex)
*
* Enter Contents of' Lo-byte input register
*
        LDAA  #$AA           1,0,1,0;1,0,1,0
        STAA  LSBS           LSBS are set to AA (Hex)
*
        LDX   #MSBS          Stack pointer at 1st byte to send via Port B
        LDY   #$1000         Stack pointer at on-chip registers
*
* Clear DAC output to zero
*
        BCLR  PORTC,Y $04    Assert CLR/
        BSET  PORTC,Y $04    De-assert CLR/
*
* Loading input buffer latches
*
        BSET  PORTC,Y $01    Set hi-byte register load
TFRLP   LDAA  0,X            Get a byte to transfer via Port B
        STAA  PORTB          Write data to input register
        INX                  Increment counter to next byte for transfer
        CPX   #LSBS+1        Are we done yet ?
        BEQ   DUMP           If yes, update DAC output
        BCLR  PORTC,Y $01    Latch hi-byte register and set lo-byte register
                             load
        BRA   TFRLP
*
```

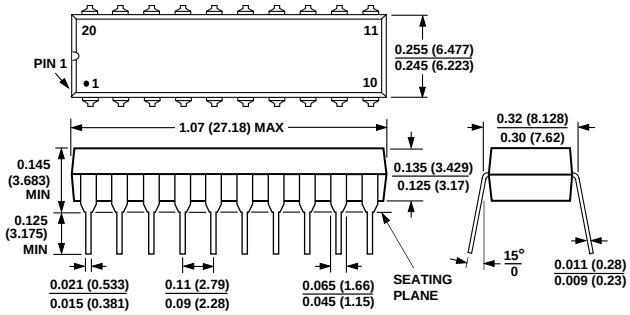
DAC8562–M68HC11 Interface Program Source Code (Continued)

```
* Update DAC output with contents of input registers
*
DUMP    BCLR  PORTC,Y $02    Assert CE/
        BSET  PORTC,Y $02    Latch DAC register
*
        PULA                 When done, restore registers X, Y & A
        PULY
        PULX
        RTS                  ** Return to Main Program **
```

OUTLINE DIMENSIONS

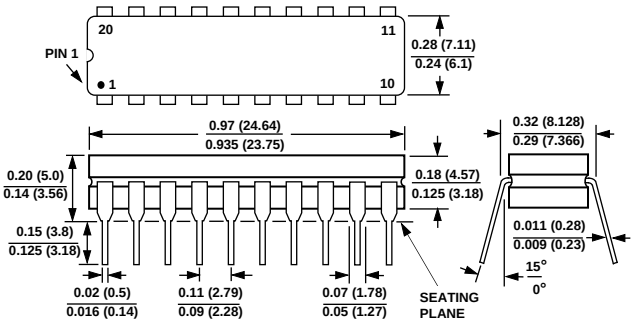
Dimensions shown in inches and (mm).

20-Pin Plastic DIP (P-Suffix)



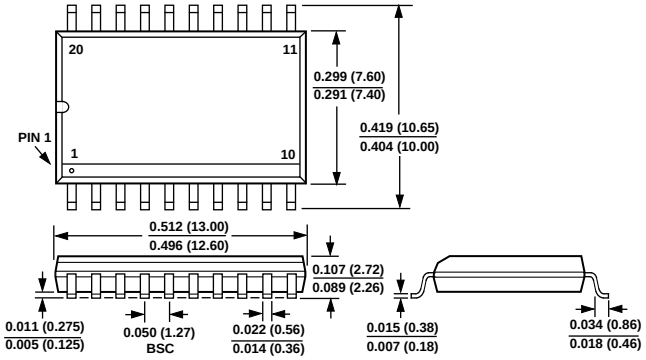
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42.

20-Pin Cerdip (R-Suffix)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42.

20-Lead SOIC (S-Suffix)



C1713–24–10/92

PRINTED IN U.S.A.

National Semiconductor

November 1995

MM54HC14/MM74HC14
Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

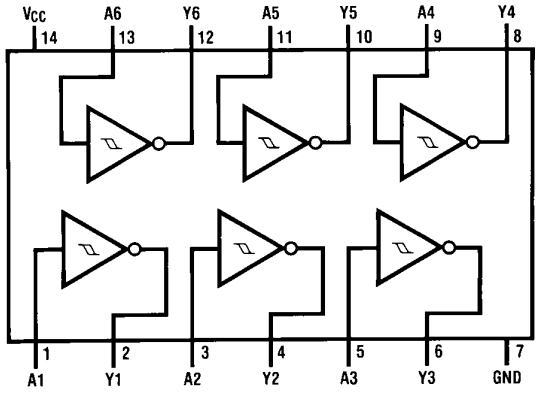
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC}=4.5V$

Connection and Schematic Diagrams

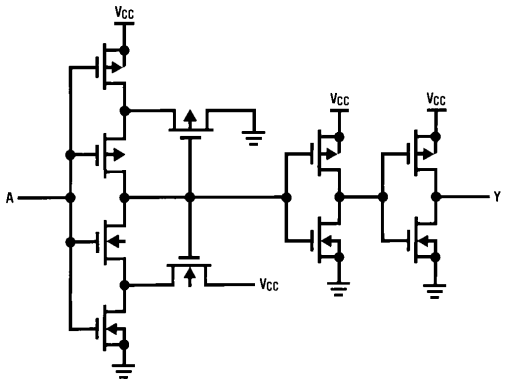
Dual-In-Line Package



TL/F/5105–1

Top View

Order Number MM54HC14 or MM74HC14



TL/F/5105–2

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	V
			4.5V	2.7	2.0	2.0	V
			6.0V	3.2	3.0	3.0	V
		Maximum	2.0V	1.2	1.5	1.5	V
			4.5V	2.7	3.15	3.15	V
			6.0V	3.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	V
			4.5V	1.8	0.9	0.9	V
			6.0V	2.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	V
			4.5V	1.8	2.2	2.2	V
			6.0V	2.2	3.0	3.0	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	V
			4.5V	0.9	0.4	0.4	V
			6.0V	1.0	0.5	0.5	V
		Maximum	2.0V	0.5	1.0	1.0	V
			4.5V	0.9	1.4	1.4	V
			6.0V	1.0	1.5	1.5	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\|$ = 20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IL} $\|I_{OUT}\|$ = 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\|$ = 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\|$ = 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

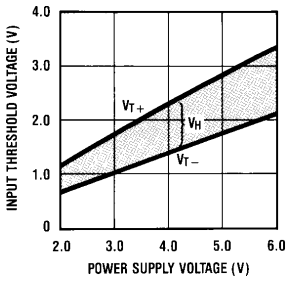
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

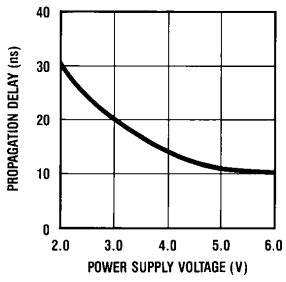
Typical Performance Characteristics

Input Threshold, V_T+, V_T-, vs Power Supply Voltage



TL/F/5105–3

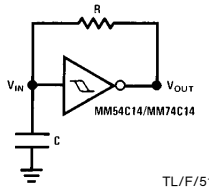
Propagation Delay vs Power Supply



TL/F/5105–4

Typical Applications

Low Power Oscillator



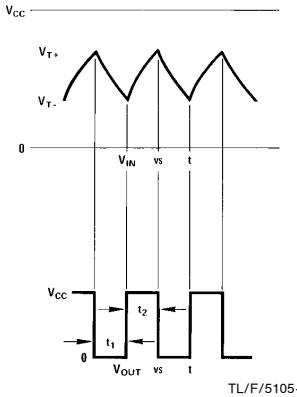
TL/F/5105–5

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$$

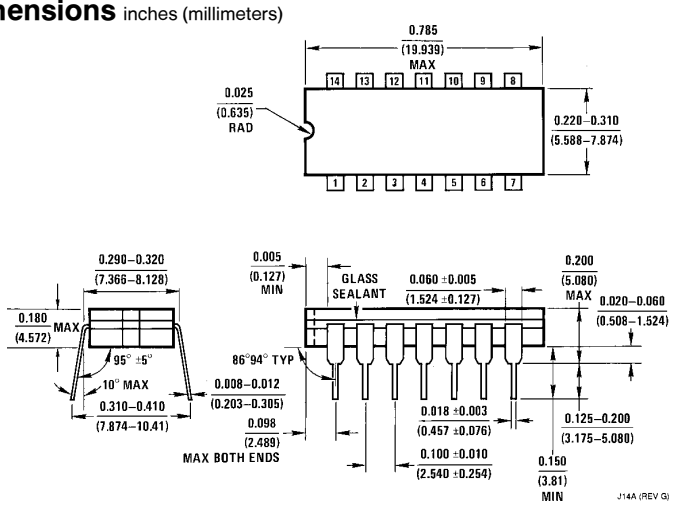
$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC}-V_{T-})}{V_{T-}(V_{CC}-V_{T+})}}$$

Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$

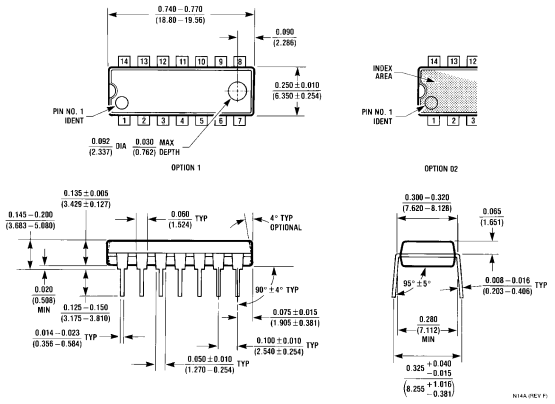


TL/F/5105–6

Physical Dimensions inches (millimeters)



Dual-In-Line Package (J)
Order Number MM54HC14J or MM74HC14J
NS Package J14A



Dual-In-Line Package (N)
Order Number MM74HC14N
NS Package N14A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRELIMINARY

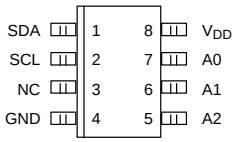
DALLAS SEMICONDUCTOR

DS1624
Digital Thermometer and Memory

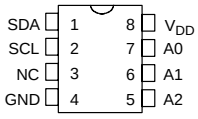
FEATURES

- Temperature measurements require no external components
- Measures temperatures from –55°C to +125°C in 0.03125°C increments. Fahrenheit equivalent is –67°F to 257°F in 0.05625°F increments
- Temperature is read as a 13–bit value (two byte transfer)
- Converts temperature to digital word in 200 ms, typical
- 256 bytes of E^2 memory on board for storing information such as frequency compensation coefficients
- Data is read/written via a 2–wire serial interface (open drain I/O lines)
- Applications include temperature–compensated crystal oscillators for test equipment and radio systems
- 8–pin DIP or SOIC package

PIN ASSIGNMENT



DS1624S
8–PIN SOIC (208 MIL)
See Mech. Drawings Section



DS1624
8–PIN DIP (300 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

SDA	–	2–Wire Serial Data Input/Output
SCL	–	2–Wire Serial Clock
GND	–	Ground
A0	–	Chip Address Input
A1	–	Chip Address Input
A2	–	Chip Address Input
V_{DD}	–	Digital Power Supply (+3V– +5V)
NC	–	No Connection

DESCRIPTION

The DS1624 consists of a digital thermometer and 256 bytes of E^2 memory. The thermometer provides 13–bit temperature readings which indicate the temperature of the device. The E^2 memory allows a user to store frequency compensation coefficients for digital correction of crystal frequency due to temperature. Any other type of information may also reside in this user space.

DETAILED PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1	SDA	**Data input/output pin** for 2–wire serial communication port.
2	SCL	**Clock input/output pin** for 2–wire serial communication port.
3	NC	**No Connect**. No Internal Connection.
4	GND	**Ground pin.**
5	A2	**Address input pin.**
6	A1	**Address input pin.**
7	A0	**Address input pin.**
8	V_{DD}	**Supply Voltage** 3V to 5V input power pin.

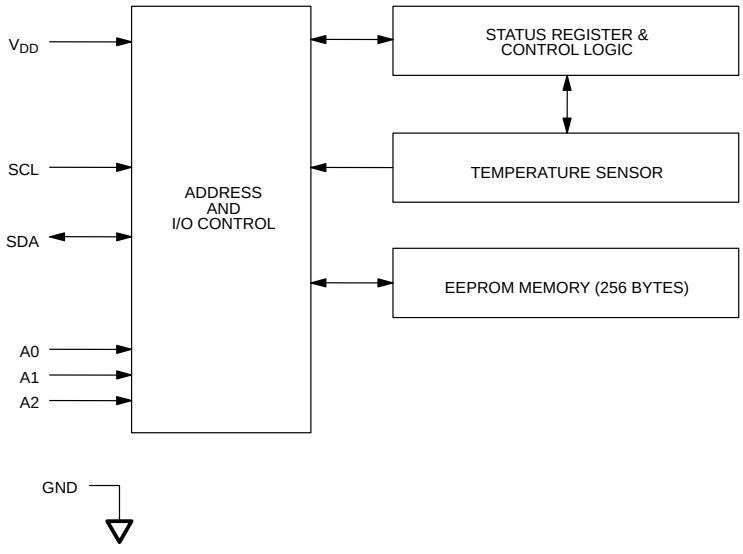
OVERVIEW

A block diagram of the DS1624 is shown in Figure 1. The DS1624 consists of two separate functional units: 1) a 256–byte nonvolatile E^2 memory, and 2) a direct–to–digital temperature sensor.

The nonvolatile memory is made up of 256 bytes of E^2 memory. This memory may be used to store any type of information the user wishes; for example, frequency compensation coefficients may be placed in this memory to allow for compensation of measured frequency depending upon the temperature at which the measurement is made. These memory locations are accessed through the 2–wire serial bus.

The direct to digital temperature sensor allows the DS1624 to measure the ambient temperature and report the temperature value in a 13–bit word, with 0.03125°C resolution. The temperature sensor and its related registers are accessed through the 2–wire serial interface.

DS1624 FUNCTIONAL BLOCK DIAGRAM Figure 1



2–WIRE SERIAL DATA BUS

The DS1624 supports a bi–directional two–wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master”. The devices that are controlled by the master are “slaves”. The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START an d STOP conditions. The DS1624 operates as a slave on the two–wire bus. Connections to the bus are made via the open–drain I/O lines SDA and SCL. The following bus protocol has been defined (See Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte–wise and each receiver acknowledges with a ninth bit.

Within the bus specifications a regular mode (100 KHz clock rate) and a fast mode (400 KHz clock rate) are defined. The DS1624 works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2–WIRE SERIAL BUS Figure 2

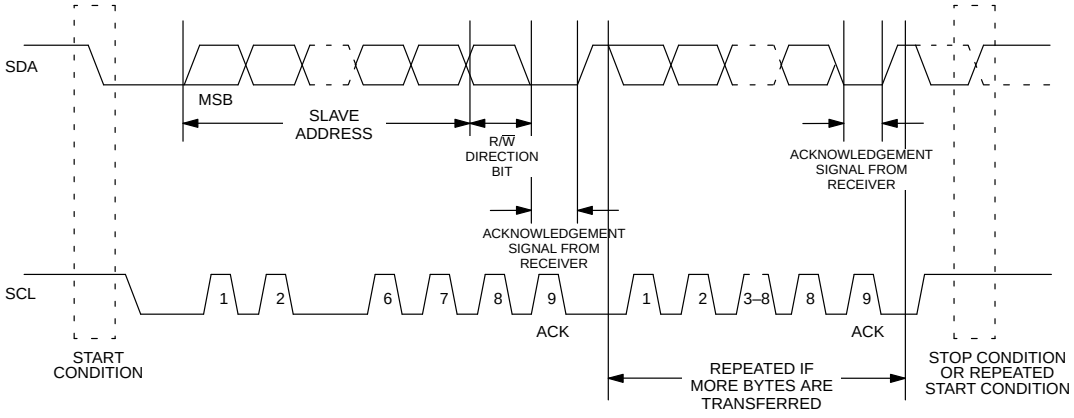


Figure 2 details how data transfer is accomplished on the two–wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1624 may operate in the following two modes:

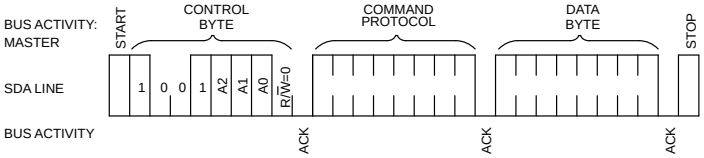
1. **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
2. **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1624 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

SLAVE ADDRESS

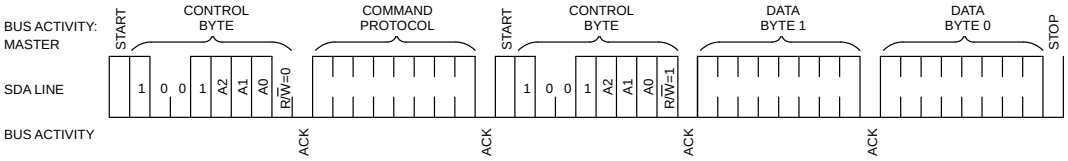
A control byte is the first byte received following the START condition from the master device. The control byte consists of a four bit control code; for the DS1624, this is set as 1001 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, A0). They are used by the master device to select which of eight devices are to be accessed. These bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1624 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1001 code and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2–WIRE SERIAL COMMUNICATION WITH DS1624 Figure 3

Write to DS1624



Read from DS1624



OPERATION–MEASURING TEMPERATURE

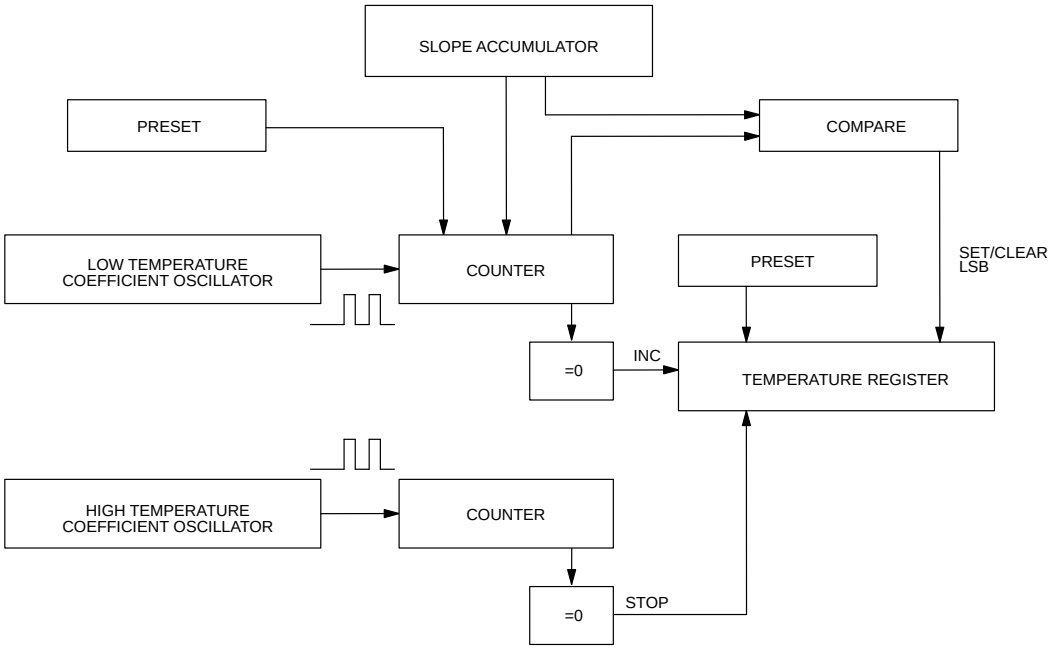
A block diagram of the DS1624 is shown in Figure 1.The DS1624 measures temperatures through the use of an on–board proprietary temperature measurement technique. A block diagram of the temperature measurement circuitry is shown in Figure 4.

The DS1624 measures temperature by counting the number of clock cycles that an oscillator with a low temperature coefficient goes through during a gate period determined by a high temperature coefficient oscillator. The counter is preset with a base count that corresponds to –55°C. If the counter reaches zero before the gate period is over, the temperature register, which is also preset to the –55°C value, is incremented, indicating that the temperature is higher than –55°C.

At the same time, the counter is then preset with a value determined by the slope accumulator circuitry. This circuitry is needed to compensate for the parabolic behavior of the oscillators over temperature. The counter is then clocked again until it reaches zero. If the gate period is still not finished, then this process repeats.

The slope accumulator is used to compensate for the nonlinear behavior of the oscillators over temperature, yielding a high resolution temperature measurement. This is done by changing the number of counts necessary for the counter to go through for each incremental degree in temperature. To obtain the desired resolution, therefore, both the value of the counter and the number of counts per degree C (the value of the slope accumulator) at a given temperature must be known.

TEMPERATURE MEASURING CIRCUITRY Figure 4



Internally, this calculation is performed by the DS1624 to provide 0.03125°C resolution. The temperature reading is provided in a 13–bit, two's complement reading by issuing READ TEMPERATURE command. Table 2 describes the exact relationship of output data to measured temperature. The data is transmitted serially through the 2–wire serial interface, MSB first. The DS1624 can measure temperature over the range of –55°C to +125°C in 0.03125°C increments. For Fahrenheit usage, a lookup table or conversion factor must be used.

TEMPERATURE/DATA RELATIONSHIPS

Table 2

TEMP	DIGITAL OUTPUT (Binary)	DIGITAL OUTPUT (Hex)
+125°C	01111101 00000000	7D00h
+25.0625°C	00011001 00010000	1910h
+1/2°C	00000000 10000000	0080h
+0°C	00000000 00000000	0070h
–1/2°C	11111111 10000000	FF80h
–25.0625°C	11100110 11110000	E6F0h
–55°C	11001001 00000000	C900h

Since data is transmitted over the 2–wire bus MSB first, temperature data may be written to/read from the DS1624 as either a single byte (with temperature resolution of 1°C), or as two bytes, the second byte containing the value of the 5 least significant bits of the temperature reading, as shown in Table 1. Note that the remaining three bits of this byte are set to all 0's.

Note that temperature is represented in the DS1624 in terms of a 0.03125°C LSB, yielding the following 13–bit format:

MSB LSB

0	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0

= –25.0625°C

OPERATION AND CONTROL

A configuration/status register is used to determine the method of operation that the DS1624 will use in a particular application, as well as indicating the status of the temperature conversion operation.

The configuration register is defined as follows:

CONFIGURATION/STATUS REGISTER

DONE	1	0	0	1	0	1	1SHOT

where

DONE= Conversion Done bit. "1" = Conversion complete, "0" = conversion in progress.

1SHOT= One Shot Mode. If 1SHOT is "1", the DS1624 will perform one temperature conversion upon reception of the Start Convert T protocol. If 1SHOT is "0", the DS1624 will continuously perform temperature conversions. This bit is nonvolatile.

Since the configuration register is implemented in E^2, writes to the register require 10 ms to complete. After issuing a command to write to the configuration register, no further accesses to the DS1624 should be made for at least 10 ms.

OPERATION – MEMORY

BYTE PROGRAM MODE

In this mode, the master sends addresses and one data byte to the DS1624.

Following a START condition, the device code (4–bit), the slave address (3 bit), and the R/$\overline{W}$ bit, which is logic LOW, are placed onto the bus by the master. The master then sends the Access Memory protocol. This indicates to the addressed DS1624 that a byte with a word address will follow after it has generated an acknowledge bit. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the DS1624. After receiving the acknowledge of the DS1624, the master device transmits the data word to be written into the addressed memory location. The DS1624 acknowledges again and the master generates a STOP condition. This initiates the internal programming cycle of the DS1624. A repeated START condition, instead of a STOP condition, will abort the programming operation.

During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms.)

PAGE PROGRAM MODE

To program the DS1624, the master sends addresses and data to the DS1624 which is the slave. This is done by supplying a START condition followed by the 4–bit device code, the 3–bit slave address, and the R/$\overline{W}$ bit which is defined as a logic LOW for a write. The master then sends the Access Memory protocol. This indicates to the addressed slave that a word address will follow so the slave outputs the acknowledge pulse to the master during the ninth clock pulse. When the word address is received by the DS1624, it is placed in the address pointer defining which memory location is to be written. The DS1624 will generate an acknowledge after every 8–bits received and store them consecutively in an 8–byte RAM until a STOP condition is detected which initiates the internal programming cycle.

A repeated START condition, instead of a STOP condition, will abort the programming operation.During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms).

If more than eight bytes are transmitted by the master, the DS1624 will roll over and overwrite the data beginning with the first received byte. This does not affect erase/write cycles of the EEPROM array and is accomplished as a result of only allowing the address register's bottom three bits to increment while the upper five bits remain unchanged.

If the master generates a STOP condition after transmitting the first data word, byte programming mode is entered.

READ MODE

In this mode, the master is reading data from the DS1624 E^2 memory. The master first provides the slave address to the device, with R/$\overline{W}$ set to 0. The master then sends the Access Memory protocol, and, after receiving an acknowledge, then provides the word address, which is the address of the memory location at which it wishes to begin reading. Note that while this is a read operation, the address pointer must first be written. During this period the DS1624 generates acknowledge bits as defined in the appropriate section.

The master now generates another START condition and transmits the slave address again, except this time the R/$\overline{W}$ bit is set to 1, to put the DS1624 in read mode. After the DS1624 generates the acknowledge bit, it then outputs the data from the addressed location on the SDA pin, increments the address pointer and, if it receives an acknowledge from the master, will transmit the next consecutive byte. This autoincrement sequence is only aborted when the master sends a STOP condition instead of an acknowledge. When the address pointer reaches the end of the 256–byte memory space (address FFh), it will increment from the end of the memory back to the first location of the memory (address 00h).

COMMAND SET

Data and control information is read from and written to the DS1624 in the format shown in Figure 3. To write to the DS1624, the master will issue the slave address of the DS1624, and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1624 will issue an acknowledge, and then the master may send data to the DS1624. If the DS1624 is to be read, the master must send the command protocol as before, and then issue a repeated START condition and the control byte again, this time with the R/$\overline{W}$ bit set to 1 to allow reading of the data from the DS1624. The command set for the DS1624 as shown in Table 3 is as follows:

Access Memory [17h]

This command instructs the DS1624 to access its E^2 memory. After issuing this command, the next data byte is the value of the word address to be accessed. See OPERATION–MEMORY section for detailed explanations of the use of this protocol and data format following it.

Access Config [ACh]

If R/$\overline{W}$ is 0, this command writes to the configuration register. After issuing this command, the next data byte is value to be written into the configuration register. If R/$\overline{W}$ is 1, the next data byte read is the value store d in the configuration register.

Read Temperature [AAh]

This command reads the last temperature conversion result. The DS1624 will send two bytes, in the format described earlier, which are the contents of this register.

Start Convert T [EEh]
This command begins a temperature conversion. No further data is required. In one–shot mode, the temperature conversion will be performed and then the DS1624 will remain idle. In continuous mode, this command will initiate continuous conversions.

Stop Convert T [22h]
This command stops temperature conversion. No further data is required. This command may be used to halt a DS1624 in continuous conversion mode. After issuing this command, the current temperature measurement will be completed, and then the DS1624 will remain idle until a Start Convert T is issued to resume continuous operation.

DS1624 COMMAND SET Table 3

INSTRUCTION	DESCRIPTION	PROTOCOL	2–WIRE BUS DATA AFTER ISSUING PROTOCOL	NOTES
TEMPERATURE CONVERSION COMMANDS				
Read Temperature	Read last converted temperature value from temperature register.	AAh	<read 2 bytes data>	
Start Convert T	Initiates temperature conversion.	EEh	idle	1
Stop Convert T	Halts temperature conversion.	22h	idle	1
MEMORY COMMANDS				
Access Memory	Reads or writes to 256–byte EEPROM memory.	17h	<write data>	2
Access Config	Reads or writes configuration data to configuration register.	ACh	<write data>	2

NOTES:

1. In continuous conversion mode, a Stop Convert T command will halt continuous conversion. To restart, the Start Convert T command must be issued. In one–shot mode, a Start Convert T command must be issued for every temperature reading desired.
2. Writing to the E^2 typically requires 10 ms at room temperature. After issuing a write command, no further reads or writes should be requested for at least 10 ms.

   During the programming cycle, the DS1624 will not acknowledge any further accesses to the device until the programming cycle is complete (approximately 10 ms).

MEMORY FUNCTION EXAMPLE

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
{Command protocol for configuration register} {Start here}				
TX	RX	START	Bus Master Initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	ACh	Bus Master sends Access Config command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	00h	Bus Master sets up DS1624 for continuous conversion.	
RX	TX	ACK	DS1624 generates acknowledge bit.	2
{Command protocol for Start Convert T} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	EEh	Bus Master sends Start Convert T command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	STOP	Bus Master initiates the STOP condition.	
{Command protocol for reading the Temperature} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr, 0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	AAh	Bus Master sends Read Temp command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,1>	Bus Master sends DS1624 address: R/$\overline{W}$=1;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the MSB byte of Temperature.	
TX	RX	ACK	Bus Master generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the LSB byte of Temperature.	
TX	RX	STOP	Bus Master Initiates the STOP condition.	

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
{Command protocol for writing to EEPROM} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	17h	Bus Master sends Access Memory command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	<madr>	Bus Master sends the starting memory address.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	<data>	Bus Master sends the first byte of data.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	<data>	Bus Master sends the second byte of data.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
.	.	.	.	
.	.	.	.	
.	.	.	.	
.	.	.	.	
TX	RX	<data>	Bus Master sends the n-th byte of data.	3
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	STOP	Bus Master initiates the STOP condition.	4
{Command protocol for reading from EEPROM} {Start here}				
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,0>	Bus Master sends DS1624 address; R/$\overline{W}$=0;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	17h	Bus Master sends Access Memory command protocol.	
RX	TX	ACK	DS1624 generates acknowledge bit.	1
TX	RX	<madr>	Bus Master sends the starting memory address.	
RX	TX	ACK	DS1624 generates acknowledge bit.	
TX	RX	START	Bus Master initiates a Start condition.	
TX	RX	<cadr,1>	Bus Master sends DS1624 address: R/$\overline{W}$=1;	
RX	TX	ACK	DS1624 generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the first byte of data.	

BUS MASTER MODE	DS1624 MODE	DATA (MSB FIRST)	COMMENTS	NOTES
TX	RX	ACK	Bus Master generates acknowledge bit.	
RX	TX	<data>	DS1624 sends the second byte of data.	
TX	RX	ACK	Bus Master generates acknowledge bit.	
•	•	•	•	
•	•	•	•	
•	•	•	•	
•	•	•	•	
RX	TX	<data>	DS1624 sends the n-th byte of data.	5
TX	RX	STOP	Bus Master initiates the STOP condition.	

NOTES:

1. If this protocol follows a write and the DS1624 does not acknowledge here, restart the protocol at the Start here. If it does acknowledge, continue on.
2. Wait for write to complete (10 ms typ. 50 ms max). If DS1624 does not acknowledge the command protocol immediately following a configure register or write mem protocol, the DS1624 has not finished writing. Restart the new command protocol until the DS1624 acknowledges.
3. If n is greater than eight, the last eight bytes are the only bytes saved in memory. If the starting address is 00 and the incoming data is 00 11 22 33 44 55 66 77 88 99, the result will be mem00=88 mem01=99 mem02=22 mem03=33 mem04=44 mem05=55 mem06=66 mem07=77. The data wraps around and overwrites itself.
4. The STOP condition causes the DS1624 to initiate the write to EEPROM sequence. If a START condition comes instead of the STOP condition, the write is aborted. The data is not saved.
5. For reading, the address is incremented. If the starting address is 04h and 30 bytes of data are read out, 21h is the final address read.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	2.97	5.0	5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–55°C to +125°C; V_{DD}=2.97V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Thermometer Error	T_{ERR}	0°C to 70°C –55°C to +0°C and +70°C to +125°C	See Typical Curve		$\pm^1/_2$	°C	11
Low Level Input Voltage	V_{IL}		–0.5		$0.3V_{DD}$	V	
High Level Input Voltage	V_{IH}		$0.7V_{DD}$		V_{DD}+0.5	V	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	Fast Mode	0		50	ns	
Low Level Output Voltage	V_{OL1}	3 mA sink current	0		0.4	V	
	V_{OL2}	6 mA sink current	0		0.6	V	
Input Current each I/O Pin		$0.4<V_{I/O}<0.9V_{DD}$	–10		10	µA	2
I/O Capacitance	$C_{I/O}$				10	pF	
Active Supply Current	I_{CC}	Temperature Conversion			1000		
		E^2 Write			400	µA	3, 4
		Communica-tion Only			100		
Standby Supply Current	I_{STBY}			1	3	µA	3, 4

AC ELECTRICAL CHARACTERISTICS (–55°C to +125°C; V_{DD}=2.97V to 5.5V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Temperature Conversion Time	T_{TC}			200	500	ms	
NV Write Cycle Time	t_{WR}	0°C to 70°C		10	50	ms	10
SCL Clock Frequency	f_{SCL}	Fast Mode Standard Mode	0 0		400 100	KHz	
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode Standard Mode	1.3 4.7			µs	
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode Standard Mode	0.6 4.0			µs	5
Low Period of SCL Clock	t_{LOW}	Fast Mode Standard Mode	1.3 4.7			µs	
High Period of SCL Clock	t_{HIGH}	Fast Mode Standard Mode	0.6 4.0			µs	
Setup Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode Standard Mode	0.6 4.7			µs	
Data Hold Time	$t_{HD:DAT}$	Fast Mode Standard Mode	0 0		0.9	µs	6, 7
Data Setup Time	$t_{SU:DAT}$	Fast Mode Standard Mode	100 250			ns	8
Rise Time of both SDA and SCL Signals	t_R	Fast Mode Standard Mode	$20+0.1C_B$		300 1000	ns	9
Fall Time of both SDA and SCL Signals	t_F	Fast Mode Standard Mode	$20+0.1C_B$		300 300	ns	9
Setup time for STOP Condition	$t_{SU:STO}$	Fast Mode Standard Mode	0.6 4.0			µs	
Capacitive Load for each Bus Line	C_b				400	pF	

All values referred to V_{IH}=0.9 V_{DD} and V_{IL}=0.1 V_{DD}.

AC ELECTRICAL CHARACTERISTICS (–55°C to +125°C; V_{DD}=2.97V to 5.5V)

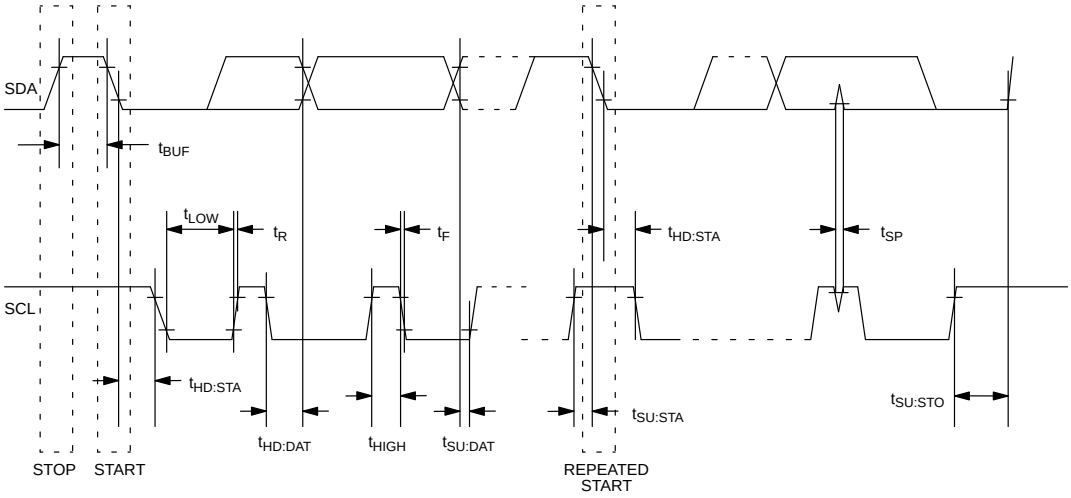
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		5		pF	

NOTES:

1. All voltages are referenced to ground.
2. I/O pins of fast mode devices must not obstruct the SDA and SCL lines if V_{DD} is switched off.
3. I_{CC} specified with SDA pin open.
4. I_{CC} specified with V_{CC} at 5.0V and SDA, SCL = 5.0V, 0°C to +70°C.

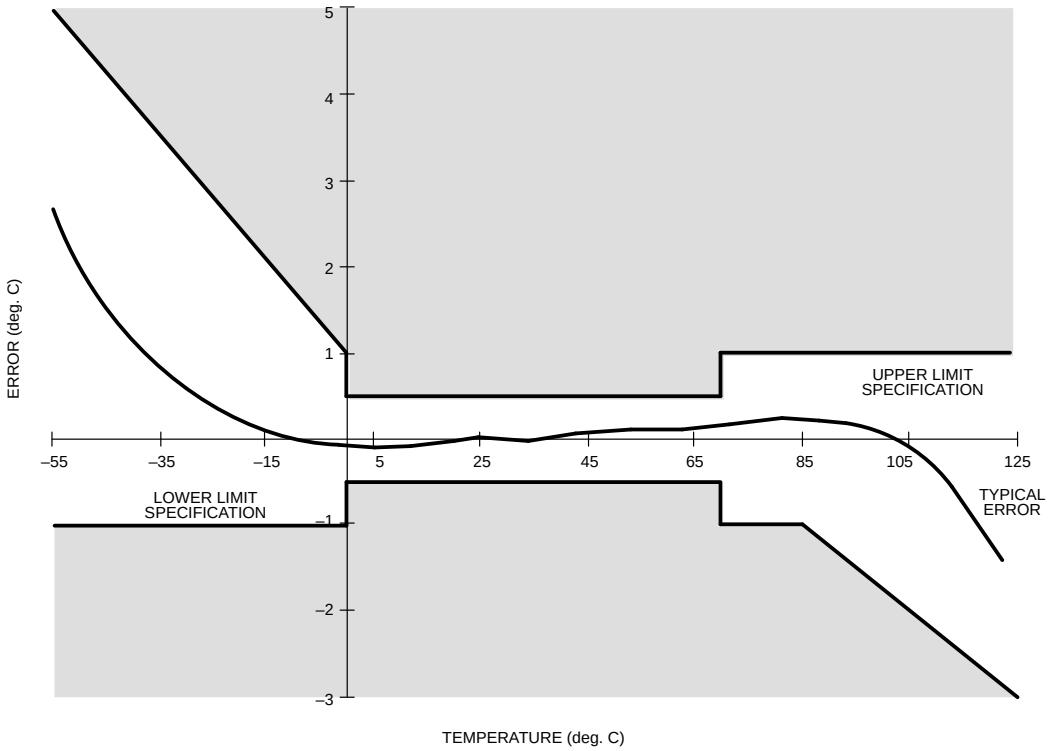
5. After this period, the first clock pulse is generated.
6. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
7. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
8. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX}+t_{SU:DAT} = 1000+250 = 1250$ ns before the SCL line is released.
9. C_b – total capacitance of one bus line in pF.
10. Writing to the nonvolatile memory should only take place in the 0°C to +70°C temperature range.
11. See Typical Curve for specification limits outside the 0°C to 70°C temperature range.

TIMING DIAGRAMS



TYPICAL PERFORMANCE CURVE

DS1624 DIGITAL THERMOMETER AND THERMOSTAT
TEMPERATURE READING ERROR



MIC2937A/29371/29372

750mA Low-Dropout Voltage Regulator

General Description

The MIC2937A family are “bulletproof” efficient voltage regulators with very low dropout voltage (typically 40mV at light loads and 300mV at 500mA), and very low quiescent current (160µA typical). The quiescent current of the MIC2937A increases only slightly in dropout, thus prolonging battery life. Key MIC2937A features include protection against reversed battery, fold-back current limiting, and automotive “load dump” protection (60V positive transient).

The MIC2937 is available in several configurations. The MIC2937A-xx devices are three pin fixed voltage regulators with 3.3V, 5V, and 12V outputs available. The MIC29371 is a fixed regulator offering logic compatible ON/OFF switching input and an error flag output. This flag may also be used as a power-on reset signal. A logic-compatible shutdown input is provided on the adjustable MIC29372, which enables the regulator to be switched on and off.

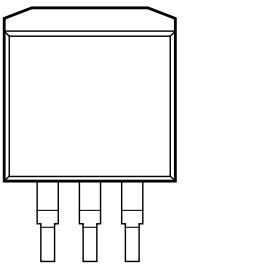
Features

- High output voltage accuracy
- Guaranteed 750mA output
- Low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Current and thermal limiting
- Input can withstand –20V reverse battery and +60V positive transients
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24V to 26V(MIC29372)
- Available in TO-220, TO-263, TO-220-5, and TO-263-5 packages.

Applications

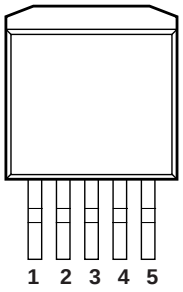
- Battery Powered Equipment
- Cellular Telephones
- Laptop, Notebook, and Palmtop Computers
- PCMCIA V_{CC} and V_{PP} Regulation/Switching
- Bar Code Scanners
- Automotive Electronics
- SMPS Post-Regulator/ DC to DC Modules
- High Efficiency Linear Power Supplies

Pin Configuration



INPUT GROUND OUTPUT

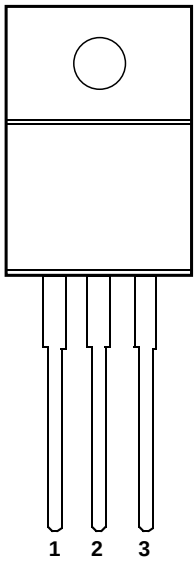
TO-263 Package
(MIC2937A-xxBU)



TO-263-5 Package
(MIC29371/29372BU)

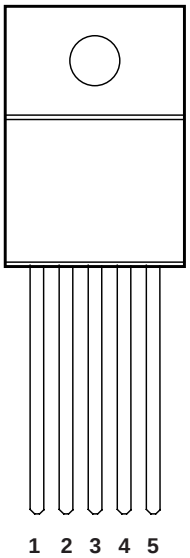
Five Lead Package Pin Functions:

	MIC29371	MIC29372
1)	Error	Adjust
2)	Input	Shutdown
3)	Ground	Ground
4)	Output	Input
5)	Shutdown	Output



INPUT GROUND OUTPUT

TO-220 Package
(MIC2937A-xxBT)



TO-220-5 Package
(MIC29371/29372BT)

The TAB is Ground on the TO-220 and TO-263 packages.

Ordering Information

Part Number	Voltage	Temperature Range*	Package
MIC2937A-3.3BU	3.3	–40°C to +125°C	TO-263-3
MIC2937A-3.3BT	3.3	–40°C to +125°C	TO-220
MIC2937A-5.0BU	5.0	–40°C to +125°C	TO-263-3
MIC2937A-5.0BT	5.0	–40°C to +125°C	TO-220
MIC2937A-12BU	12	–40°C to +125°C	TO-263-3
MIC2937A-12BT	12	–40°C to +125°C	TO-220
MIC29371-3.3BT	3.3	–40°C to +125°C	TO-220-5
MIC29371-3.3BU	3.3	–40°C to +125°C	TO-263-5
MIC29371-5.0BT	5.0	–40°C to +125°C	TO-220-5
MIC29371-5.0BU	5.0	–40°C to +125°C	TO-263-5
MIC29371-12BT	12	–40°C to +125°C	TO-220-5
MIC29371-12BU	12	–40°C to +125°C	TO-263-5
MIC29372BT	Adj	–40°C to +125°C	TO-220-5
MIC29372BU	Adj	–40°C to +125°C	TO-263-5

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power Dissipation (Note 1) ..... Internally Limited

Lead Temperature (Soldering, 5 seconds) ..... 260°C
Storage Temperature Range ..... –65°C to +150°C
Operating Junction Temperature Range
..... –40°C to +125°C
TO-220 θ_{JC} ..... 2.5°C/W
TO-263 θ_{JC} ..... 2.5°C/W
Input Supply Voltage ..... –20V to +60V
Operating Input Supply Voltage ..... 2V† to 26V
Adjust Input Voltage (Notes 9 and 10)
..... –1.5V to +26V
Shutdown Input Voltage ..... –0.3V to +30V
Error Comparator Output Voltage ..... –0.3V to +30V

† Across the full operating temperature, the minimum input voltage range for full output current is 4.3V to 26V. Output will remain in-regulation at lower output voltages and low current loads down to an input of 2V at 25°C.

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C and limits in **boldface** apply over the full operating temperature range. Unless otherwise specified, $V_{IN} = V_{OUT} + 1V$, I_L = 5mA, C_L = 10µF. The MIC29372 are programmed for a 5V output voltage, and $V_{SHUTDOWN} \leq 0.6V$ (MIC29271-xx and MIC29372 only).

Symbol	Parameter	Conditions	Min	Typical	Max	Units
V_O	Output Voltage Accuracy	Variation from factory trimmed V_{OUT}	–1 **–2**		1 **2**	%
		5mA ≤ I_L ≤ 500mA	**–2.5**		**2.5**	
		MIC2937A-12 and 29371-12 only:	–1.5 **–3**		1.5 **3**	
		5mA ≤ I_L ≤ 500mA	**–4**		**4**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coef.	(Note 2)		20	**100**	ppm/°C
		Output voltage > 10V		80	**350**	
$\frac{\Delta V_O}{V_O}$	Line Regulation	$V_{IN} = V_{OUT} + 1V$ to 26V		0.03	0.10 **0.40**	%
$\frac{\Delta V_O}{V_O}$	Load Regulation	I_L = 5 to 500mA (Note 3)		0.04	0.16 **0.30**	%
$V_{IN} – V_O$	Dropout Voltage (Note 4)	I_L = 5mA		80	150 **180**	mV
		I_L = 100mA		200		
		Output voltage > 10V		240		
		I_L = 500mA		300		
		Output voltage > 10V		420		
		I_L = 750mA		370	600 **750**	
I_{GND}	Ground Pin Current (Note 5)	I_L = 5mA		160	250 **300**	µA
		I_L = 100mA		1	2.5 **3**	mA
		I_L = 500mA		8	13 **16**	
		I_L = 750mA		15	25	
I_{GNDDO}	Ground Pin Current at Dropout (Note 5)	V_{IN} = 0.5V less than designed V_{OUT} ($V_{OUT} \geq 3.3V$) I_O = 5mA		200	**500**	µA
I_{LIMIT}	Current Limit	V_{OUT} = 0V (Note 6)		1.1	1.5 **2**	A
$\frac{\Delta V_O}{\Delta P_D}$	Thermal Regulation	(Note 7)		0.05	0.2	%/W
e_n	Output Noise Voltage (10Hz to 100kHz) I_L = 100mA	C_L = 10µF		400		µV RMS
		C_L = 100µF		260		

Electrical Characteristics (Continued)

MIC29372

Parameter	Conditions	Min	Typical	Max	Units
Reference Voltage		1.223 **1.210**	1.235	1.247 **1.260**	V V max
Reference Voltage	(Note 8)	**1.204**		**1.266**	V
Adjust Pin Bias Current			20	40 **60**	nA
Reference Voltage Temperature Coefficient	(Note 7)		20		ppm/°C
Adjust Pin Bias Current Temperature Coefficient			0.1		nA/°C
Error Comparator	**MIC29371**				
Output Leakage Current	V_{OH} = 26V		0.01	1.00 **2.00**	µA
Output Low Voltage	V_{IN} = 4.5V I_{OL} = 250µA		150	250 **400**	mV
Upper Threshold Voltage	(Note 9)	40 **25**	60		mV
Lower Threshold Voltage	(Note 9)		75	95 **140**	mV
Hysteresis	(Note 9)		15		mV
Shutdown Input	**MIC29371/MIC29372**				
Input Logic Voltage Low (ON) High (OFF)		 **2.0**	1.3	 **0.7**	V
Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 2.4V		30	50 **100**	µA
	$V_{SHUTDOWN}$ = 26V		450	600 **750**	µA
Regulator Output Current in Shutdown	(Note 10)		3	10 **20**	µA

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J\,(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

Note 2: Output voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Note 3: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Note 4: Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At low values of programmed output voltage, the minimum input supply voltage of 4.3V over temperature must be taken into account. The MIC2937A operates down to 2V of input at reduced output current at 25°C.

Note 5: Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the load current plus the ground pin current.

Note 6: The MIC2937A family features fold-back current limiting. The short circuit (V_{OUT} = 0V) current limit is less than the maximum current with normal output voltage.

Note 7: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 200mA load pulse at V_{IN} = 20V (a 4W pulse) for T = 10ms.

Note 8: $V_{REF} \le V_{OUT} \le (V_{IN} - 1\ V)$, $4.3V \le V_{IN} \le 26V$, $5mA < I_L \le 750\ mA$, $T_J \le T_{J\,MAX.}$

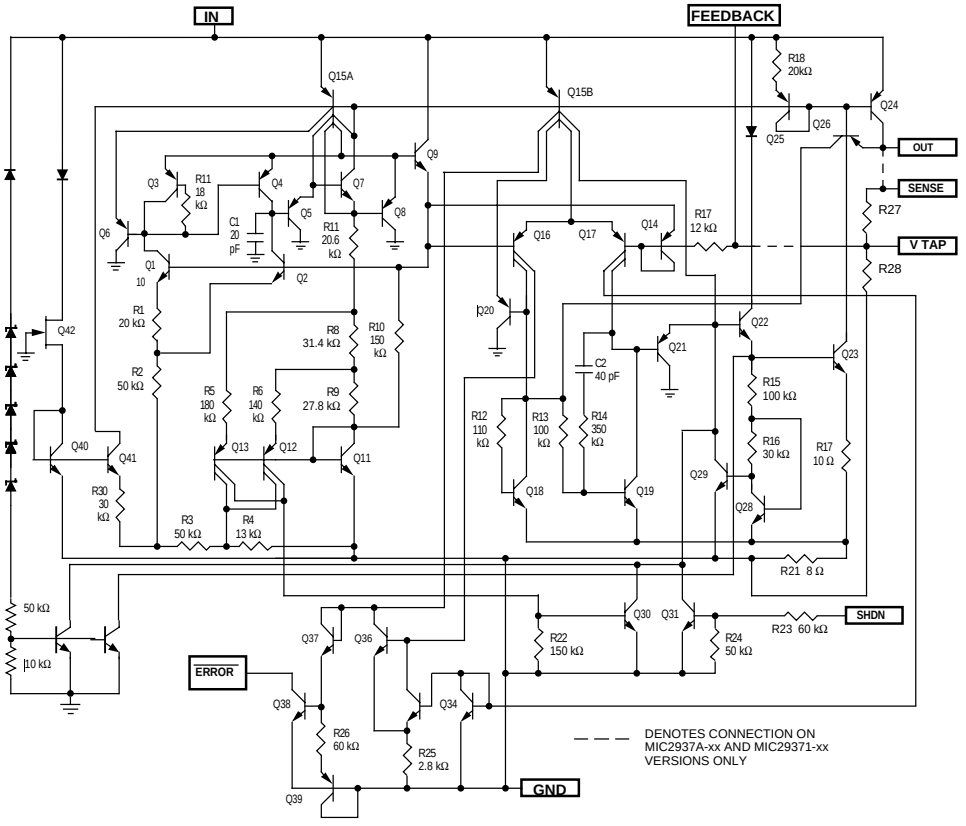
Note 9: Comparator thresholds are expressed in terms of a voltage differential at the Adjust terminal below the nominal reference voltage measured at 6V input (for a 5V regulator). To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} / V_{REF} = (R1 + R2)/R2. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by 95 mV x 5V/1.235 V = 384 mV. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.7% guaranteed.

Note 10: Circuit of Figure 3 with R1 ≥ 150kΩ. $V_{SHUTDOWN} \ge 2V$ and $V_{IN} \le 26V$, V_{OUT} = 0.

Note 11: When used in dual supply systems where the regulator load is returned to a negative supply, the output voltage must be diode clamped to ground.

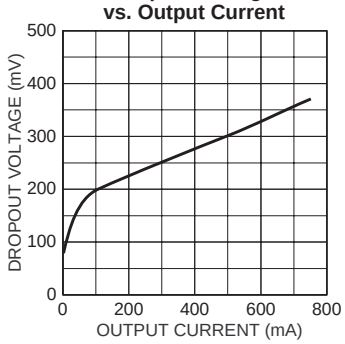
Note 12: Maximum positive supply voltage of 60V must be of limited duration (< 100ms) and duty cycle (≤ 1%). The maximum continuous supply voltage is 26V.

Schematic Diagram

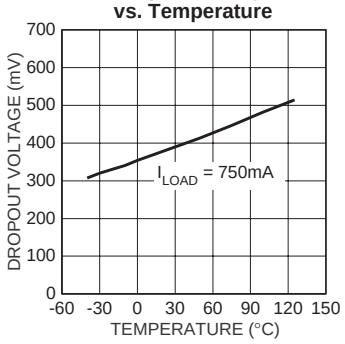


Typical Characteristics

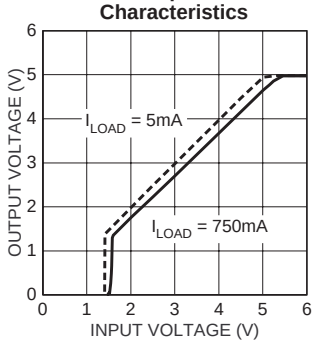
Dropout Voltage vs. Output Current



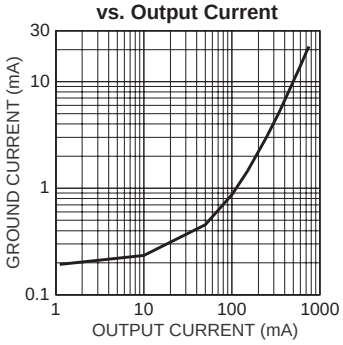
Dropout Voltage vs. Temperature



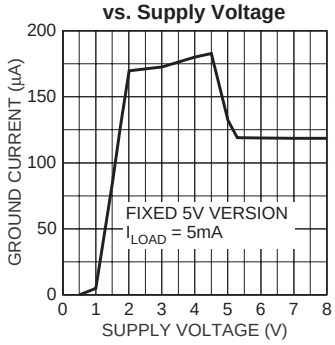
Dropout Characteristics



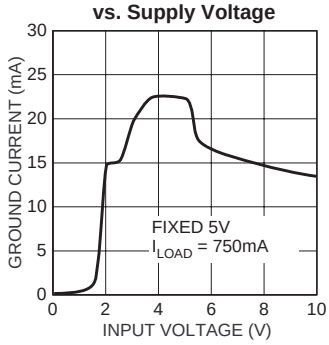
Ground Current vs. Output Current



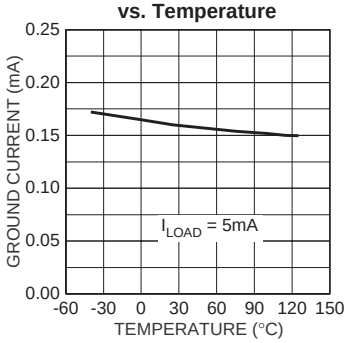
Ground Current vs. Supply Voltage



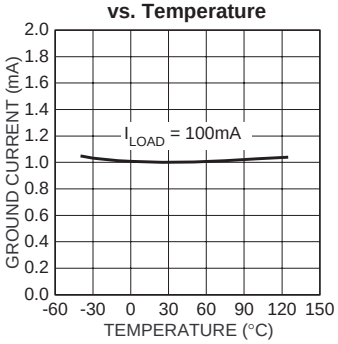
Ground Current vs. Supply Voltage



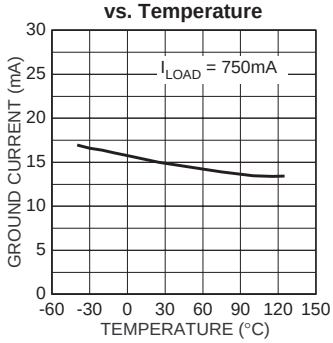
Ground Current vs. Temperature



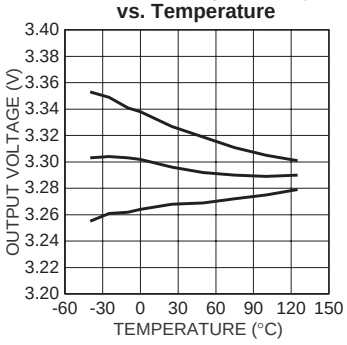
Ground Current vs. Temperature



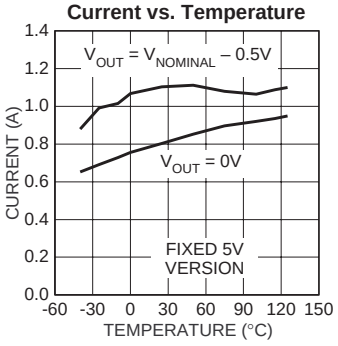
Ground Current vs. Temperature



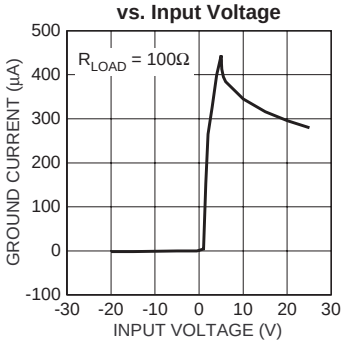
Fixed 3.3V Output Voltage vs. Temperature



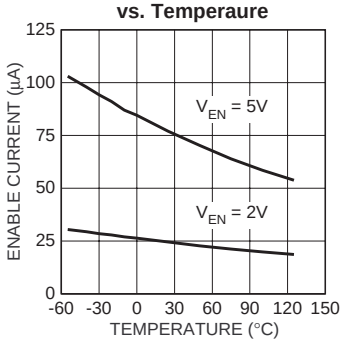
Short Circuit and Maximum Current vs. Temperature



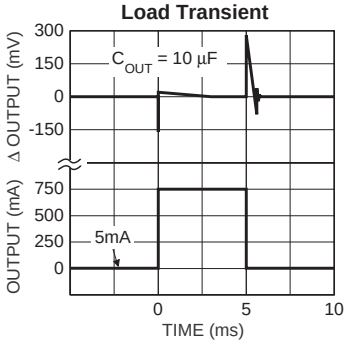
Ground Current vs. Input Voltage



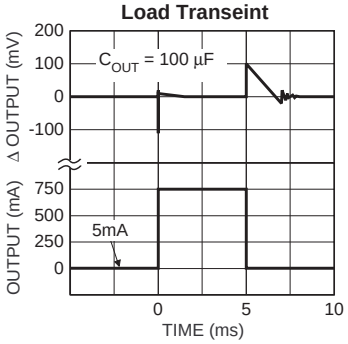
MIC29371/2 Shutdown Current vs. Temperaure



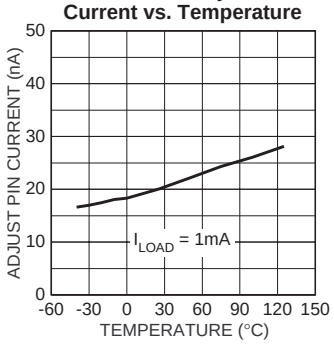
Load Transient



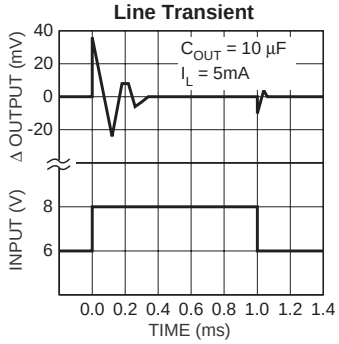
Load Transeint



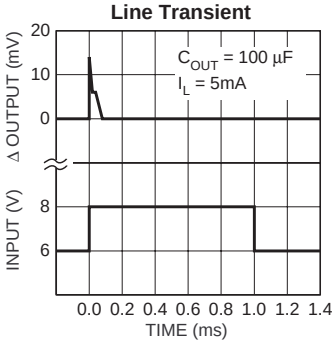
MIC29372/3 Adjust Pin Current vs. Temperature



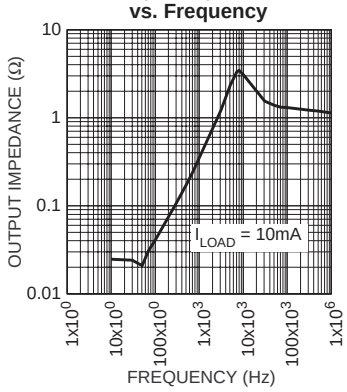
Line Transient



Line Transient



Output Impedance vs. Frequency



Applications Information

External Capacitors

A 10µF (or greater) capacitor is required between the MIC2937A output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about –30°C, so solid tantalums are recommended for operation below –25°C. The important parameters of the capacitor are an effective series resistance of about 5Ω or less and a resonant frequency above 500kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.5µF for current below 10mA or 0.15µF for currents below 1 mA. Adjusting the MIC29372 to voltages below 5V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 750mA load at 1.23V output (Output shorted to Adjust) a 22µF (or greater) capacitor should be used.

The MIC2937A/29371 will remain in regulation with a minimum load of 5mA. When setting the output voltage of the MIC29372 version with external resistors, the current through these resistors may be included as a portion of the minimum load.

A 0.1µF capacitor should be placed from the input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Error Detection Comparator Output (MIC29371)

A logic low output will be produced by the comparator whenever the MIC29371 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 75mV divided by the 1.235V reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC29371. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage,extremely high input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC29371 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which V_{OUT} = 4.75). Since the MIC29371's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approximately 4.75V) does not vary with load.

The error comparator has an NPN open-collector output which requires an external pull-up resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 250µA, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1MΩ. The resistor is not required if this output is unused.

Programming the Output Voltage (MIC29372)

The MIC29372 may programmed for any output voltage between its 1.235V reference and its 26V maximum rating. An external pair of resistors is required, as shown in Figure 3.

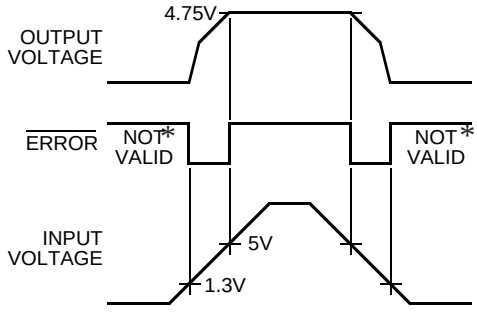
The complete equation for the output voltage is

$$V_{OUT} = V_{REF} \times \{ 1 + R_1/R_2 \} - |I_{FB}| R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the Adjust pin bias current, nominally 20nA. The minimum recommended load current of 1µA forces an upper limit of 1.2MΩ on the value of R_2, if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a –2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1. For better accuracy, choosing R_2 = 100k reduces this error to 0.17% while increasing the resistor program current to 12µA. Since the MIC29372 typically draws 100µA at no load with SHUTDOWN open-circuited, this is a negligible addition.

Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is relatively inefficient, as increasing the capacitor from 1µF to 220µF only decreases the noise from 430µV to 160μV_{RMS} for a 100kHz bandwidth at 5V output. Noise can be reduced by a factor of four with the adjustable



* SEE APPLICATIONS INFORMATION

Figure 1. $\overline{\text{ERROR}}$ Output Timing

regulators with a bypass capacitor across R_1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{BYPASS} \cong \frac{1}{2\pi R_1 \bullet 200\ Hz}$$

or about 0.01µF. When doing this, the output capacitor must be increased to 10µF to maintain stability. These changes reduce the output noise from 430µV to 100μV_{RMS} for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Automotive Applications

The MIC2937A is ideally suited for automotive applications for a variety of reasons. It will operate over a wide range of input voltages with very low dropout voltages (40mV at light loads), and very low quiescent currents (100µA typical). These features are necessary for use in battery powered systems, such as automobiles. It is a "bulletproof" device with the ability to survive both reverse battery (negative transients up to 20V below ground), and load dump (positive transients up to 60V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

Typical Applications

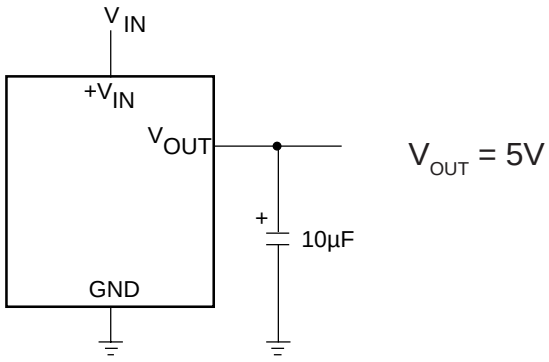


Figure 2. MIC2937A-5.0 Fixed +5V Regulator

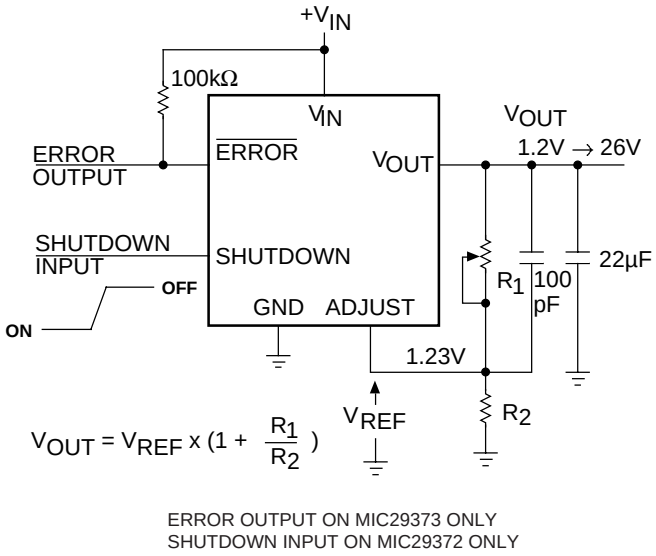
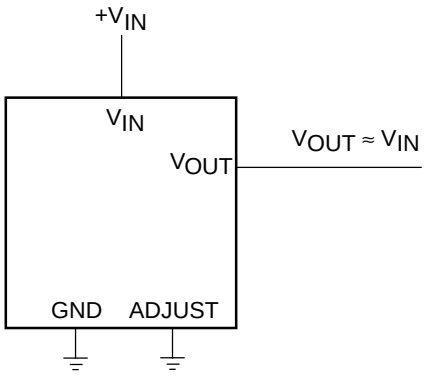
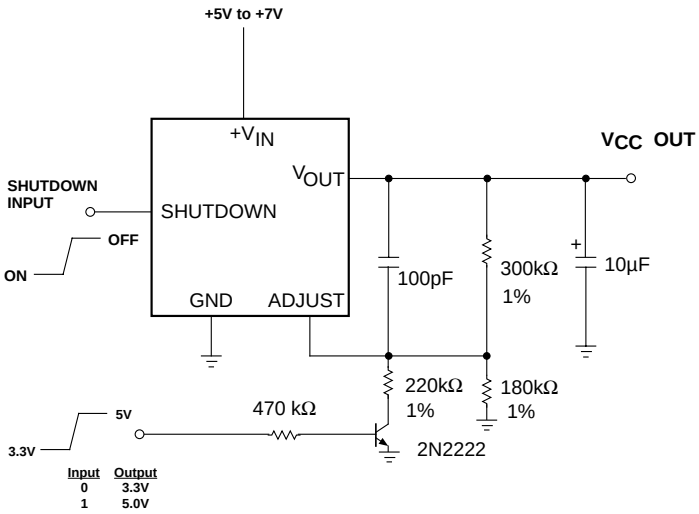


Figure 3. MIC29372 Adjustable Regulator



*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40mV TO 400mV, DEPENDING ON LOAD CURRENT.

Figure 4. MIC29372 Wide Input Voltage Range Current Limiter



SHUTDOWN PIN LOW= ENABLE OUTPUT. Q1 ON = 3.3V, Q1 OFF = 5.0V.

Figure 5. MIC29372 5.0V or 3.3V Selectable Regulator with Shutdown.

500mA Negative Low Dropout Micropower Regulator

FEATURES

- Stable with Wide Range of Output Capacitors
- **Operating Current: 45μA**
- Shutdown Current: 10μA
- **Adjustable Current Limit**
- Positive or Negative Shutdown Logic
- **Low Voltage Linear Dropout Characteristics**
- Fixed 5V and Adjustable Versions
- Tolerates Reverse Output Voltage

APPLICATIONS

- Analog Systems
- Modems
- Instrumentation
- A/D and D/A Converters
- Interface Drivers
- Battery-Powered Systems

DESCRIPTION

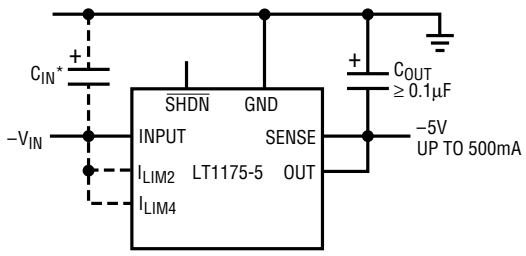
The LT®1175 is a negative micropower low dropout regulator. It features 45μA quiescent current, dropping to 10μA in shutdown. A new reference amplifier topology gives precision DC characteristics along with the ability to maintain good loop stability with an extremely wide range of output capacitors. Very low dropout voltage and high efficiency are obtained with a unique power transistor anti-saturation design. Adjustable and fixed 5V versions are available.

Several new features make the LT1175 very user-friendly. The Shutdown pin can interface directly to either positive or negative logic levels. Current limit is user-selectable at 200mA, 400mA, 600mA and 800mA. The output can be forced to reverse voltage without damage or latchup. Unlike some earlier designs, the increase in quiescent current during a dropout condition is actively limited.

The LT1175 has complete blowout protection with current limiting, power limiting and thermal shutdown. Special attention was given to the problem of high temperature operation with micropower operating currents, preventing output voltage rise under no-load conditions. The LT1175 is available in 8-pin PDIP and SO packages, 3-lead SOT-223 as well as 5-pin surface mount DD and through-hole TO-220 packages. The 8-pin SO package is specially constructed for low thermal resistance.

TYPICAL APPLICATION

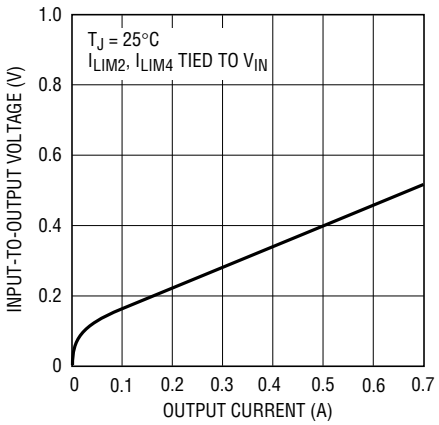
Typical LT1175 Connection



*C_{IN} IS NEEDED ONLY IF REGULATOR IS MORE THAN 6" FROM INPUT SUPPLY CAPACITOR. SEE APPLICATIONS INFORMATION SECTION FOR DETAILS

1175 TA01

Minimum Input-to-Output Voltage

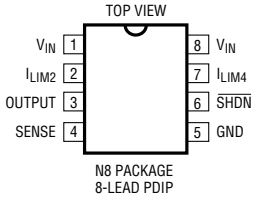


1175 TA02

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Transient 1 sec, Note 10) 25V
Input Voltage (Continuous)..... 20V
Input-to-Output Differential Voltage (Note 11)..... 20V
5V Sense Pin (with Respect to GND Pin)..... 2V, –10V
ADJ Sense Pin
(with Respect to Output Pin) ..... 20V, –0.5V
5V Sense Pin
(with Respect to Output Pin) ..... 20V, – 7V
Output Reverse Voltage 2V
$\overline{SHDN}$ Pin to GND Pin Voltage ..... 15V, –20V
$\overline{SHDN}$ Pin to V_{IN} Pin Voltage ..... 30V, –5V
Operating Junction Temperature Range
LT1175C..... 0°C to 125°C
LT1175I ..... –40°C to 125°C
Ambient Operating Temperature Range
LT1175C..... 0°C to 70°C
LT1175I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

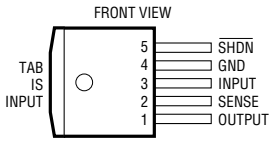


N8 PACKAGE
8-LEAD PDIP

θ_{JA} = 80°C/W TO 120°C/W DEPENDING ON PC BOARD LAYOUT

ORDER PART NUMBER

LT1175CN8
LT1175CN8-5
LT1175IN8
LT1175IN8-5

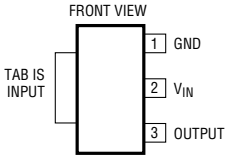


Q PACKAGE
5-LEAD PLASTIC DD

θ_{JA} = 27°C/W TO 60°C/W DEPENDING ON PC MOUNTING. SEE DATA SHEET FOR DETAILS

ORDER PART NUMBER

LT1175CQ
LT1175CQ-5
LT1175IQ
LT1175IQ-5

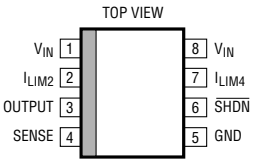


ST PACKAGE
3-LEAD PLASTIC SOT-223

θ_{JA} = 50°C/W WITH BACKPLANE AND 10cm² TOPSIDE LAND SOLDERED TO TAB

ORDER PART NUMBER

LT1175CST-5
LT1175IST-5



S8 PACKAGE
8-LEAD PLASTIC SO

θ_{JA} = 60°C/W TO 100°C/W DEPENDING ON PC BOARD LAYOUT

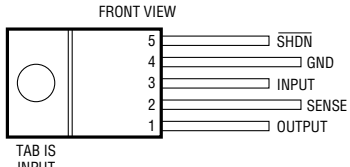
PINS 1, 8 ARE INTERNALLY CONNECTED TO DIE ATTACH PADDLE FOR HEAT SINKING. ELECTRICAL CONTACT CAN BE MADE TO EITHER PIN. FOR BEST THERMAL RESISTANCE, PINS 1, 8 SHOULD BE CONNECTED TO AN EXPANDED LAND THAT IS OVER AN INTERNAL OR BACKSIDE PLANE. SEE APPLICATIONS INFORMATION

ORDER PART NUMBER

LT1175CS8
LT1175CS8-5
LT1175IS8
LT1175IS8-5

S8 PART MARKING

1175 1175I
11755 1175I5



T PACKAGE
5-LEAD PLASTIC TO-220

θ_{JA} = 50°C/W, θ_{JC} = 5°C/W

ORDER PART NUMBER

LT1175CT
LT1175CT-5
LT1175IT
LT1175IT-5

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{OUT} = 5V; V_{IN} = 7V, I_{OUT} = 0, V_{SHDN} = 3V, I_{LIM2} and I_{LIM4} tied to V_{IN}, T_J = 25°C, unless otherwise noted. To avoid confusion with "min" and "max" as applied to negative voltages, all voltages are shown as absolute values except where polarity is not obvious.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Sense Voltage	Adjustable Part		3.743	3.8	3.857	V
	Fixed 5V Part		4.93	5.0	5.075	V
Output Voltage Initial Accuracy	Adjustable, Measured at 3.8V Sense			0.5	1.5	%
	Fixed 5V			0.5	1.5	%
Output Voltage Accuracy (All Conditions)	$V_{IN} – V_{OUT}$ = 1V to V_{IN} = 20V, I_{OUT} = 0A to 500mA P = 0 to P_{MAX}, $T_J = T_{MIN}$ to T_{MAX} (Note 2)	●		1.5	2.5	%
Quiescent Input Supply Current	$V_{IN} – V_{OUT} \leq 12V$			45	65	µA
		●			80	µA

ELECTRICAL CHARACTERISTICS

V_{OUT} = 5V; V_{IN} = 7V, I_{OUT} = 0, V_{SHDN} = 3V, I_{LIM2} and I_{LIM4} tied to V_{IN}, T_J = 25°C, unless otherwise noted. To avoid confusion with "min" and "max" as applied to negative voltages, all voltages are shown as absolute values except where polarity is not obvious.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GND Pin Current Increase with Load (Note 3)		●		10	20	µA/mA
Input Supply Current in Shutdown	V_{SHDN} = 0V			10	20	µA
		●			25	µA
Shutdown Thresholds (Note 8)	Either Polarity on $\overline{\text{Shutdown}}$ Pin	●	0.8		2.5	V
$\overline{\text{Shutdown}}$ Pin Current (Note 1)	V_{SHDN} = 0V to 10V (Flows Into Pin)	●		4	8	µA
	V_{SHDN} = –15V to 0V (Flows Into Pin)			1	4	µA
Output Bleed Current in Shutdown (Note 5)	V_{OUT} = 0V, V_{IN} = 15V			0.1	1	µA
		●		1	5	µA
Sense Pin Input Current	(Adjustable Part Only, Current Flows Out of Pin)	●		75	150	nA
	(Fixed Voltage Only, Current Flows Out of Pin)	●		12	20	µA
Dropout Voltage (Note 6)	I_{OUT} = 25mA	●		0.1	0.2	V
	I_{OUT} = 100mA	●		0.18	0.26	V
	I_{OUT} = 500mA	●		0.5	0.7	V
	I_{LIM2} Open, I_{OUT} = 300mA	●		0.33	0.5	V
	I_{LIM4} Open, I_{OUT} = 200mA	●		0.3	0.45	V
	I_{LIM2}, I_{LIM4} Open, I_{OUT} = 100mA	●		0.26	0.45	V
Current Limit (Note 10)	V_{IN} – V_{OUT} = 1V to 12V	●	520	800		mA
	I_{LIM2} Open	●	390	600		mA
	I_{LIM4} Open	●	260	400		mA
	I_{LIM2}, I_{LIM4} Open	●	130	200		mA
Line Regulation (Note 9)	V_{IN} – V_{OUT} = 1V to V_{IN} = 25V	●		0.003	0.015	%/V
Load Regulation (Note 4, 9)	I_{OUT} = 0 to 500mA	●		0.1	0.35	%
Thermal Regulation	P = 0 to P_{MAX} (Notes 2, 7) 5-Pin Packages			0.04	0.1	%/W
	8-Pin Packages			0.1	0.2	%/W
Output Voltage Temperature Drift	T_J = 25°C to T_{JMIN}, or 25°C to T_{JMAX}			0.25	1.25	%

The ● denotes specifications which apply over the operating temperature range.

Note 1: $\overline{\text{Shutdown}}$ pin maximum positive voltage is 30V with respect to $-V_{IN}$ and 15V with respect to GND. Maximum negative voltage is –20V with respect to ground and –5V with respect to $-V_{IN}$.

Note 2: P_{MAX} = 1.5W for 8-pin packages, and 6W for 5-pin packages. This power level holds only for input-to-output voltages up to 12V, beyond which internal power limiting may reduce power. See Guaranteed Current Limit curve in Typical Performance Characteristics section. Note that all conditions must be met.

Note 3: Ground pin current increases because of power transistor base drive. At low input-to-output voltages (< 1V) where the power transistor is in saturation, Ground pin current will be slightly higher. See Typical Performance Characteristics.

Note 4: With I_{LOAD} = 0, at T_J > 125°C, power transistor leakage could increase higher than the 10µA to 25µA drawn by the output divider or fixed voltage Sense pin, causing the output to rise above the regulated value. To prevent this condition, an internal active pull-up will automatically turn on, but supply current will increase.

Note 5: This is the current required to pull the output voltage to within 1V of ground during shutdown.

Note 6: Dropout voltage is measured by setting the input voltage equal to the normal regulated output voltage and measuring the difference between V_{IN} and V_{OUT}. For currents between 100mA and 500mA, with both I_{LIM} pins tied to V_{IN}, maximum dropout can be calculated from V_{DO} = 0.15 + 1.1Ω (I_{OUT}).

Note 7: Thermal regulation is a change in the output voltage caused by die temperature gradients, so it is proportional to chip power dissipation. Temperature gradients reach final value in less than 100ms. Output voltage changes after 100ms are due to absolute die temperature changes and reference voltage temperature coefficient.

Note 8: The lower limit of 0.8V is guaranteed to keep the regulator in shutdown. The upper limit of 2.5V is guaranteed to keep the regulator active. Either polarity may be used, referenced to Ground pin.

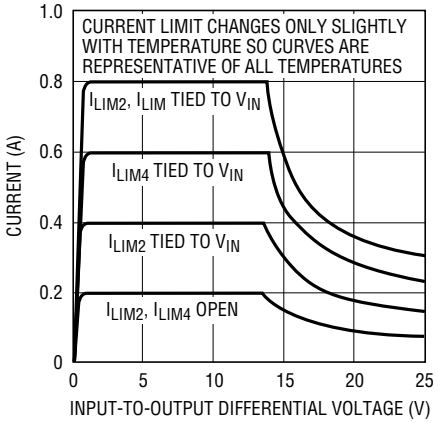
Note 9: Load and line regulation are measured on a pulse basis with pulse width of 20ms or less to keep chip temperature constant. DC regulation will be affected by thermal regulation (Note 7) and chip temperature changes. Load regulation specification also holds for currents up to the specified current limit when I_{LIM2} or I_{LIM4} are left open.

Note 10: Current limit is reduced for input-to-output voltage above 12V. See the graph in Typical Performance Characteristics for guaranteed limits above 12V.

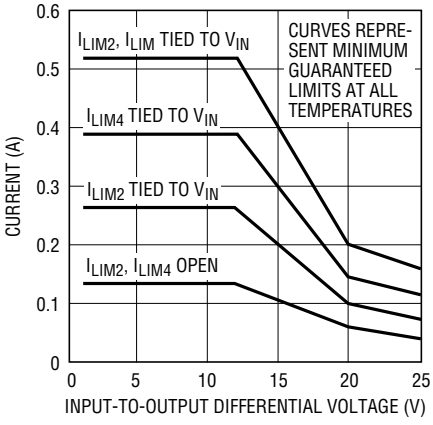
Note 11: Operating at very large input-to-output differential voltages (>15V) with load currents less than 5mA requires an output capacitor with an ESR greater than 1Ω to prevent low level output oscillations.

TYPICAL PERFORMANCE CHARACTERISTICS

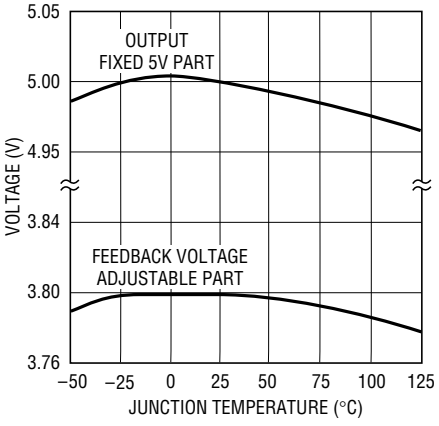
Typical Current Limit Characteristics



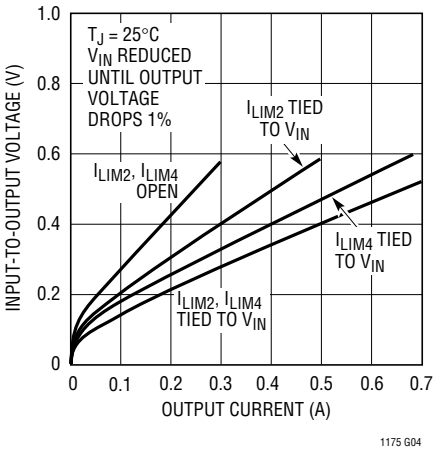
Guaranteed Current Limit



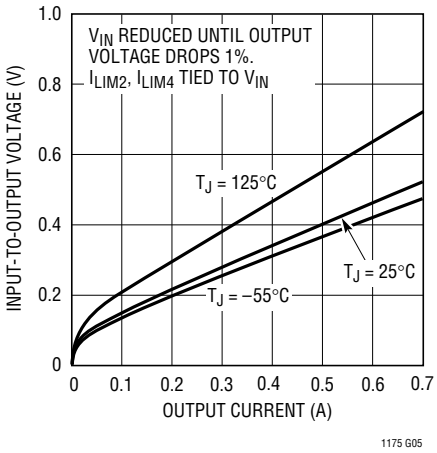
Output Voltage Temperature Drift



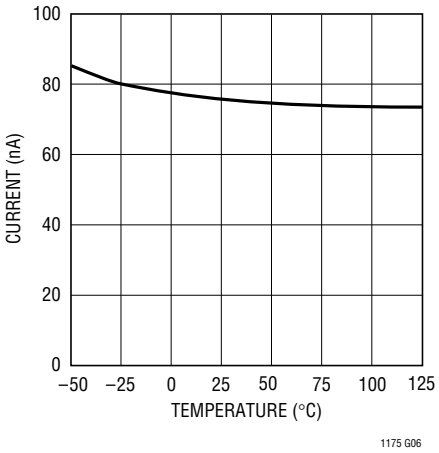
Minimum Input-to-Output Voltage



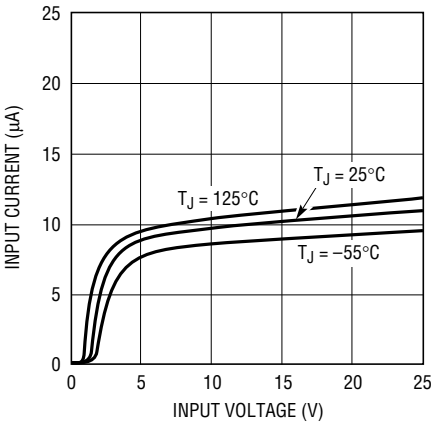
Minimum Input-to-Output Voltage



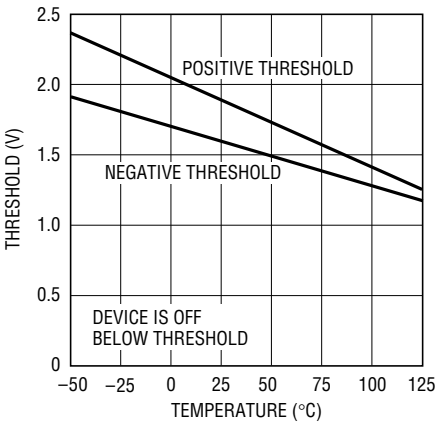
Sense Bias Current (Adjustable Part)



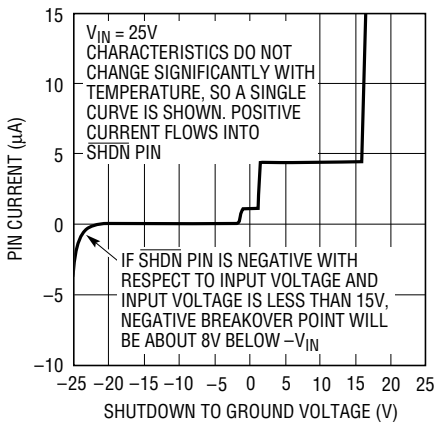
Shutdown Input Current



Shutdown Thresholds

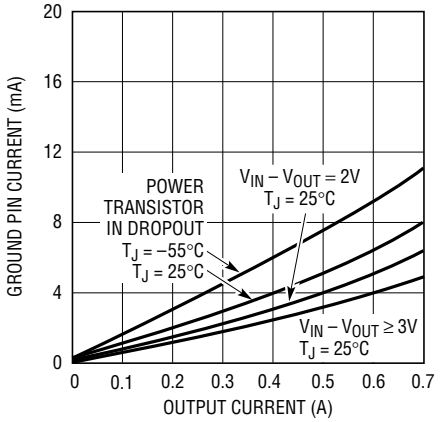


$\overline{\text{Shutdown}}$ Pin Characteristics



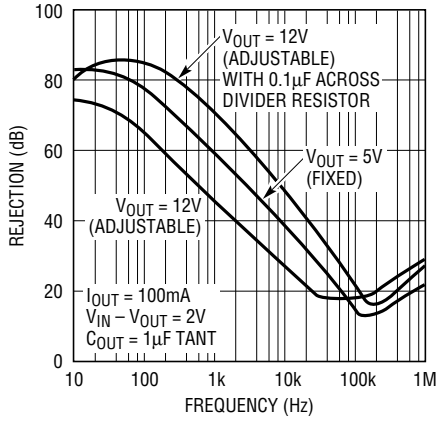
TYPICAL PERFORMANCE CHARACTERISTICS

Ground Pin Current



1175 G10

Ripple Rejection



RIPPLE REJECTION IS RELATIVELY INDEPENDENT OF INPUT VOLTAGE AND LOAD FOR CURRENTS BETWEEN 25mA AND 500mA. LARGER OUTPUT CAPACITORS DO NOT IMPROVE REJECTION FOR FREQUENCIES BELOW 50kHz. AT VERY LIGHT LOADS, REJECTION WILL IMPROVE WITH LARGER OUTPUT CAPACITORS 1175 G11

PIN FUNCTIONS

SENSE Pin: The Sense pin is used in the adjustable version to allow custom selection of output voltage, with an external divider set to generate 3.8V at the Sense pin. Input bias current is typically 75nA flowing out of the pin. Maximum forced voltage on the Sense pin is 2V and –10V with respect to Ground pin.

The fixed 5V version utilizes the Sense pin to give true Kelvin connections to the load or to drive an external pass transistor for higher output currents. Bias current out of the 5V Sense pin is approximately 12µA. Separating the Sense and Output pins also allows for a new loop compensation technique described in the Applications Information section.

$\overline{\text{SHDN}}$ Pin: The $\overline{\text{Shutdown}}$ pin is specially configured to allow it to be driven from either positive voltage logic or with negative only logic. Forcing the $\overline{\text{Shutdown}}$ pin 2V either above or below the Ground pin will turn the regulator on. This makes it simple to connect directly to positive logic signals for active low shutdown. If no positive voltages are available, the $\overline{\text{Shutdown}}$ pin can be driven below the Ground pin to turn the regulator on. *When left open, the $\overline{\text{Shutdown}}$ pin will default low to a regulator "on" condition*. For all voltages below absolute maximum ratings, the $\overline{\text{Shutdown}}$ pin draws only a few microamperes of current (see Typical Performance Characteristics). Maximum voltage on the $\overline{\text{Shutdown}}$ pin is 15V, –20V with respect to the Ground pin and 35V, –5V with respect to the negative Input pin.

I_{LIM} Pins: The two Current Limit pins are emitter sections of the power transistor. When left open, they float several hundred millivolts above the negative input voltage. When shorted to the input voltage, they increase current limit by a minimum of 200mA for I_{LIM2} and 400mA for I_{LIM4}. These pins must be connected only to the input voltage, either directly or through a resistor.

OUTPUT Pin: The Output pin is the collector of the NPN power transistor. It can be forced to the input voltage, to ground or up to 2V positive with respect to ground without damage or latchup (see Output Voltage Reversal in Applications Information section). The LT1175 has foldback current limit, so maximum current at the Output pin is a function of input-to-output voltage. See Typical Performance Characteristics.

GND Pin: The Ground pin has a quiescent current of 45µA at zero load current, increasing by approximately 10µA per mA of output current. At 500mA output current, Ground pin current is about 5mA. Current flows into the Ground pin.

APPLICATIONS INFORMATION

Note to Reader: To avoid confusion when working with negative voltages (is –6V more or less than –5V?), I have decided to treat the LT1175 as if it were a positive regulator and express all voltages as positive values, both in text and in formulas. If you do the same and simply add a negative sign to the eventual answer, confusion should be avoided. Please don't give me a hard time about "preciseness" or "correctness." I have to field phone calls from around the world and this is my way of dealing with a multitude of conventions. Thanks for your patience.

Setting Output Voltage

The LT1175 adjustable version has a feedback sense voltage of 3.8V with a bias current of approximately 75nA flowing out of the Sense pin. To avoid output voltage errors caused by this current, the output divider string (see Figure 1) should draw about 25μA. Table 1 shows suggested resistor values for a range of output voltages. The second part of the table shows resistor values which draw only 10μA of current. Output voltage error caused by bias current with the lower valued resistors is about 0.4% maximum and with the higher values, about 1% maximum. A formula is also shown for calculating the resistors for any output voltage.

Table 1

OUTPUT VOLTAGE	R1 I_{DIV} = 25μA	R2 NEAREST 1%	R1 I_{DIV} = 10μA	R2 NEAREST 1%
5V	150k	47.5k	383k	121k
6V	150k	86.6k	383k	221k
8V	150k	165k	383k	422k
10V	150k	243k	383k	619k
12V	150k	324k	383k	825k
15V	150k	442k	383k	1.13M

$$R1 = \frac{3.8V}{I_{DIV}}$$

$$R2 = \frac{R1\left(V_{OUT} - 3.8V\right)}{3.8V} \quad \left(\text{Simple formula}\right)$$

$$R2 = \frac{R1\left(V_{OUT} - 3.8V\right)}{3.8V + R1\left(I_{FB}\right)} \quad \left(\begin{array}{l}\text{Taking Sense pin bias}\\ \text{current into account}\end{array}\right)$$

I_{DIV} = Desired divider current

The LT1175-5 is a fixed 5V design with the Sense pin acting as a Kelvin connection to the output. Normally the Sense pin and the Output pin are connected directly together, either close to the regulator or at the remote load point.

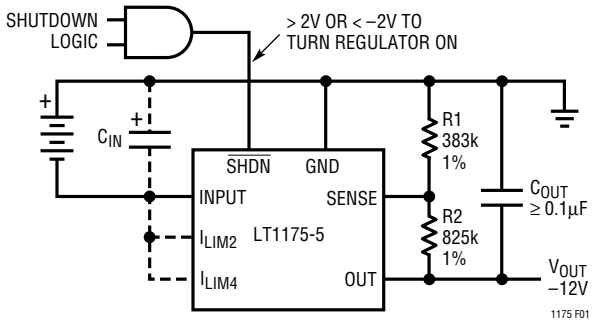


Figure 1. Typical LT1175 Adjustable Connection

Setting Current Limit

The LT1175 uses two I_{LIM} pins to set current limit (typical) at 200mA, 400mA, 600mA or 800mA. The corresponding minimum guaranteed currents are 130mA, 260mA, 390mA and 520mA. This allows the user to select a current limit tailored to his specific application and prevents the situation where short-circuit current is many times higher than full-load current. Problems with input supply overload or excessive power dissipation in a faulted load are prevented. Power limiting in the form of foldback current limit is built-in and reduces current limit as a function of input-to-output voltage differential for differentials exceeding 14V. See the graph in Typical Performance Characteristics. The LT1175 is guaranteed to be blowout-proof regardless of current limit setting. The power limiting combined with thermal shutdown protects the device from destructive junction temperatures under all load conditions.

Shutdown

In shutdown, the LT1175 draws only about 10μA. Special circuitry is used to minimize increases in shutdown current at high temperatures, but a slight increase is seen above 125°C. One option *not taken* was to actively pull down on the output during shutdown. This means that the output will fall slowly after shutdown is initiated, at a rate determined by load current plus the 12μA internal load, and the size of the output capacitor. Active pull-down is

APPLICATIONS INFORMATION

normally a good thing when the regulator is used by itself, but it prevents the user from shutting down the regulator when a second power source is connected to the LT1175 output. If active output pull-down is needed in shutdown, it can be added externally with a depletion mode PFET as shown in Figure 2. Note that the maximum pinch-off voltage of the PFET must be less than the positive logic high level to ensure that the device is completely off when the regulator is active. The Motorola J177 device has 300Ω on resistance for zero gate source voltage.

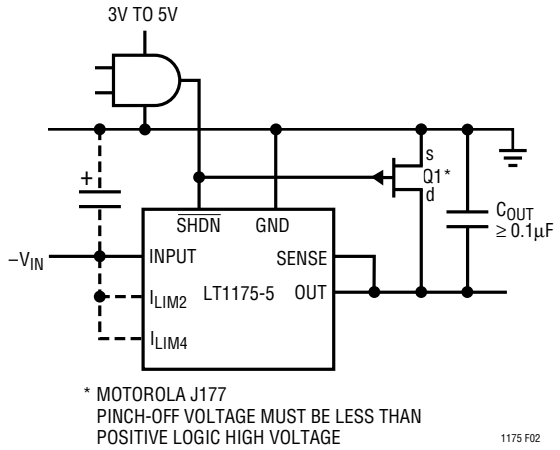


Figure 2. Active Output Pull-Down During Shutdown

Minimum Dropout Voltage

Dropout voltage is the minimum voltage required between input and output to maintain proper output regulation. For older 3-terminal regulator designs, dropout voltage was typically 1.5V to 3V. The LT1175 uses a saturating power transistor design which gives much lower dropout voltage, typically 100mV at light loads and 450mV at full load. Special precautions were taken to ensure that this technique does not cause quiescent supply current to be high under light load conditions. When the regulator input voltage is too low to maintain a regulated output, the pass transistor is driven hard by the error amplifier as it tries to maintain regulation. The current drawn by the driver transistor could be tens of milliamperes even with little or no load on the output. This indeed was the case for older IC designs that did not actively limit driver current when the power transistor saturated. The LT1175 uses a new antisaturation technique that prevents high driver current, yet allows the power transistor to approach its theoretical saturation limit.

Output Capacitor

Several new regulator design techniques are used to make the LT1175 extremely tolerant of output capacitor selection. Like most low dropout designs which use a collector or drain of the power transistor to drive the output node, the LT1175 uses the output capacitor as part of the overall loop compensation. Older regulators generally required the output capacitor to have a minimum value of 1µF to 100µF, a *maximum* ESR (Effective Series Resistance) of 0.1Ω to 1Ω and a *minimum* ESR in the range of 0.03Ω to 0.3Ω. These restrictions usually could be met only with good quality solid tantalum capacitors. Aluminum capacitors have problems with high ESR unless much higher values of capacitance are used (physically large). The ESR of ceramic or film capacitors was too *low*, which made the capacitance/ESR zero frequency too high to maintain phase margin in the regulator. Even with optimum capacitors, loop phase margin was very low in previous designs when output current was low. These problems led to a new design technique for the LT1175 error amplifier and internal frequency compensation as shown in Figure 3.

A conventional regulator loop consists of error amplifier A1, driver transistor Q2 and power transistor Q1. Added to this basic loop are secondary loops generated by Q3 and C_F. A DC negative feedback current fed into the error amplifier through Q3 and R_N causes overall loop current gain to be very low at light load currents. This is not a problem because very little gain is needed at light loads. In addition to low gain, the parasitic pole frequency at Q2 base is extended by the DC feedback. The combination of these two effects dramatically improves loop phase margin at light loads and makes the loop tolerant of large ESR in the output capacitor. With heavy loads, loop phase and gain are not nearly as troublesome and large negative feedback could degrade regulation. The logarithmic behavior of the base emitter voltage of Q1 reduces Q3 negative feedback at heavy loads to prevent poor regulation.

In a conventional design, even with the nonlinear feedback, poor loop phase margin would occur at medium to heavy loads if the ESR of the output capacitor fell below

APPLICATIONS INFORMATION

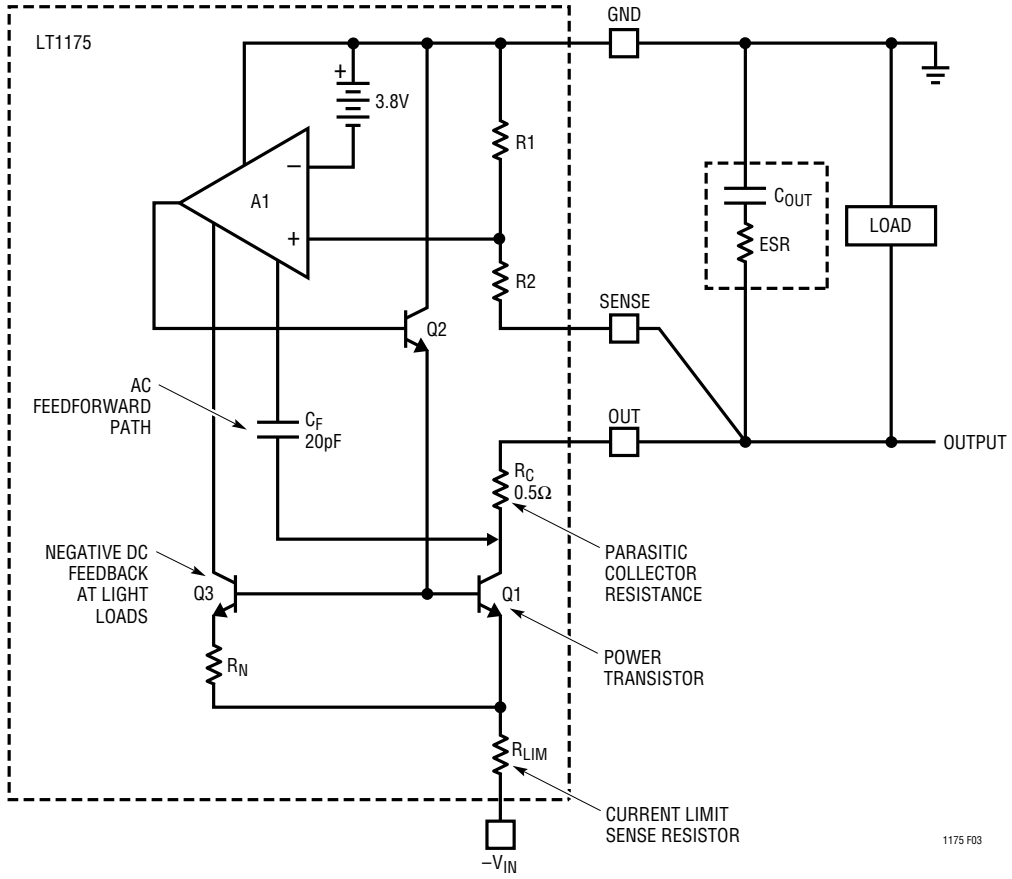


Figure 3

0.3Ω. This condition can occur with ceramic or film capacitors which often have an ESR under 0.1Ω. With previous designs, the user was forced to add a real resistor in series with the capacitor to guarantee loop stability. The LT1175 uses a unique AC feedforward technique to eliminate this problem. C_F is a conventional feedforward capacitor often used in regulators to cancel the pole formed by the output capacitor. It would normally be connected from the regulated output node to the feedback node at the R1/R2 junction or to an internal node on the amplifier as shown. In this case, however, the capacitor is connected to the internal structure of the power transistor. R_C is the unavoidable parasitic collector resistance of the power transistor. Access to the node at the bottom of R_C is available only in monolithic structures where Kelvin connections can be made to the NPN buried collector layer. The loop now responds as if R_C were in series with the output capacitor and good loop stability is achieved even with extremely low ESR in the output capacitor.

The end result of all this attention to loop stability is that the output capacitor used with the LT1175 can range in value from 0.1μF to hundreds of microfarads, with an ESR from 0Ω to 10Ω. This range allows the use of ceramic, solid tantalum, aluminum and film capacitors over a wide range of values.

The optimum output capacitor type for the LT1175 is still solid tantalum, but there is considerable leeway in selecting the exact unit. If large load current transients are expected, larger capacitors with lower ESR may be needed to control worst case output variation during transients. If transients are not an issue, the capacitor can be chosen for small physical size, low price, etc. Concerns about surge currents in tantalum capacitors are not an issue for the output capacitor because the LT1175 limits inrush current to well below the level which can cause capacitor damage. Surges caused by shorting the regulator output are also not a problem because tantalum capacitors do not fail

APPLICATIONS INFORMATION

during a "shorting out" surge, only during a "charge up" surge.

The output capacitor should be located within several inches of the regulator. If remote sensing is used, the output capacitor can be located at the remote sense node, but the Ground pin of the regulator should also be connected to the remote site. The basic rule is to keep Sense and Ground pins close to the output capacitor, regardless of where it is.

Operating at very large input-to-output differential voltages (> 5V) with load currents less than 5mA requires an output capacitor with an ESR greater than 1Ω to prevent low level output oscillations.

Input Capacitor

The LT1175 requires a separate input bypass capacitor only if the regulator is located more than six inches from the raw supply output capacitor. A 1μF or larger tantalum capacitor is suggested for all applications, but if low ESR capacitors such as ceramic or film are used for the output *and* input capacitors, the input capacitor should be at least three times the value of the output capacitor. If a solid tantalum or aluminum electrolytic output capacitor is used, the input capacitor is very noncritical.

High Temperature Operation

The LT1175 is a micropower design with only 45μA quiescent current. This could make it perform poorly at high temperatures (>125°C), where power transistor leakage might exceed the output node loading current (5μA to 15μA). To avoid a condition where the output voltage drifts uncontrolled high during a high temperature no-load condition, the LT1175 has an active load which turns on when the output is pulled above the nominal regulated voltage. This load absorbs power transistor leakage and maintains good regulation. There is one downside to this feature, however. If the output is pulled high deliberately, as it might be when the LT1175 is used as a backup to a slightly higher output from a primary regulator, the LT1175 will act as an unwanted load on the primary regulator. Because of this, the active pull-down is deliberately "weak." It can be modeled as a 2k resistor in series with an internal clamp voltage when the regulator output is being pulled high. If a 4.8V output is pulled to 5V, for instance, the load on the primary regulator would be (5V – 4.8V)/2kΩ = 100μA. This also means that if the internal pass transistor leaks 50μA, the output voltage will be (50μA)(2kΩ) = 100mV high. This condition will not occur under normal operating conditions, but could occur immediately after an output short circuit had overheated the chip.

Thermal Considerations

The LT1175 is available in a special 8-pin surface mount package which has pins 1 and 8 connected to the die attach paddle. This reduces thermal resistance when pins 1 and 8 are connected to expanded copper lands on the PC board. Table 2 shows thermal resistance for various combinations of copper lands and backside or internal planes. Table 2 also shows thermal resistance for the 5-pin DD surface mount package and the 8-pin DIP and package.

Table 2. Package Thermal Resistance (°C/W)

LAND AREA	DIP	ST	SO	Q
Minimum	140	90	100	60
Minimum with Backplane	110	70	80	50
1cm^2 Top Plane with Backplane	100	64	75	35
10cm^2 Top Plane with Backplane	80	50	60	27

To calculate die temperature, maximum power dissipation or maximum input voltage, use the following formulas with correct thermal resistance numbers from Table 2. For through-hole TO-220 applications use θ_{JA} = 50°C/W without a heat sink and θ_{JA} = 5°C/W + heat sink thermal resistance when using a heat sink.

$$\text{Die Temp} = T_A + \theta_{JA}\left(V_{IN} - V_{OUT}\right)\left(I_{LOAD}\right)$$

$$\text{Maximum Power Dissipation} = \frac{T_{MAX} - T_A}{\theta_{JA}}$$

$$\text{Maximum Input Voltage for Thermal Considerations} = \frac{T_{MAX} - T_A}{\theta_{JA}\left(I_{LOAD}\right)} + V_{OUT}$$

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T_A = Maximum ambient temperature

T_{MAX} = Maximum LT1175 die temperature (125°C for commercial and industrial grades)

θ_{JA} = LT1175 thermal resistance, junction to ambient

V_{IN} = Maximum continuous input voltage at maximum load current

I_{LOAD} = Maximum load current

Example: LT1175S8 with I_{LOAD} = 200mA, V_{OUT} = 5V, V_{IN} = 7V, T_A = 60°C. Maximum die temperature for the LT1175S8 is 125°C. Thermal resistance from Table 2 is found to be 80°C/W.

Die Temperature = 60 + 80 (0.2A)(8 – 5) = 108°C

$$\text{Maximum Power Dissipation} = \frac{125-60}{80} = 0.81\text{W}$$

$$\text{Maximum Continuous Input Voltage (for Thermal Considerations)} = \frac{125-60}{80(0.2)} + 5 = 9\text{V}$$

Output Voltage Reversal

The LT1175 is designed to tolerate an output voltage reversal of up to 2V. Reversal might occur, for instance, if the output was shorted to a positive 5V supply. This would almost surely destroy IC devices connected to the negative output. Reversal could also occur during start-up if the positive supply came up first and loads were connected between the positive and negative supplies. *For these reasons, it is always good design practice to add a reverse biased diode from each regulator output to ground to limit output voltage reversal*. The diode should be rated to handle full negative load current for start-up situations, or the short-circuit current of the positive supply if supply-to-supply shorts must be tolerated.

Input Voltage Lower Than Output

Linear Technology's positive low dropout regulators LT1121 and LT1129, will not draw large currents if the input voltage is less than the output. These devices use a lateral PNP power transistor structure that has 40V emitter base breakdown voltage. *The LT1175, however, uses an NPN power transistor structure that has a parasitic diode between the input and output of the regulator*. Reverse voltages between input and output above 1V will damage the regulator if large currents are allowed to flow. Simply disconnecting the input source with the output held up will not cause damage even though the input-to-output voltage will become slightly reversed.

High Frequency Ripple Rejection

The LT1175 will sometimes be powered from switching regulators that generate the unregulated or quasi-regulated input voltage. This voltage will contain high frequency ripple that must be rejected by the linear regulator. Special care was taken with the LT1175 to maximize high frequency ripple rejection, but as with any micropower design, rejection is strongly affected by ripple frequency. The graph in the Typical Performance Characteristics section shows 60dB rejection at 1kHz, but only 15dB rejection at 100kHz for the 5V part. Photographs in Figures 4a and 4b show actual output ripple waveforms with square wave and triwave input ripple.

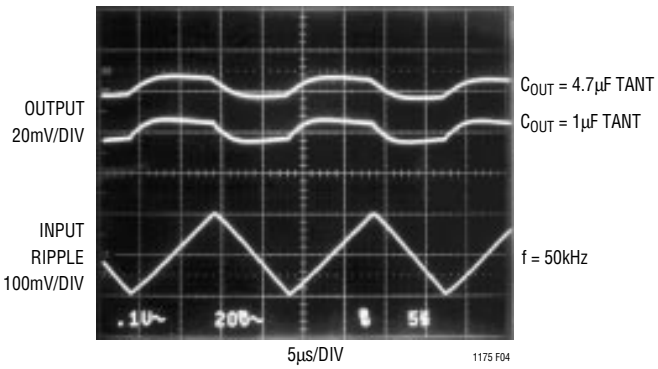


Figure 4a.

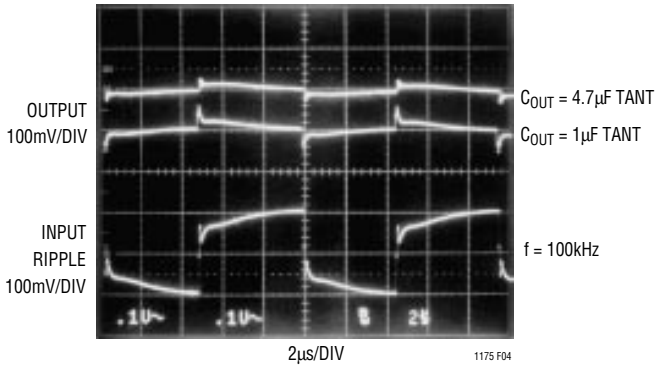


Figure 4b.

APPLICATIONS INFORMATION

To estimate regulator output ripple under different conditions, the following general comments should be helpful:

1. Output ripple at high frequency is only weakly affected by load current or output capacitor size for medium to heavy loads. At very light loads (<10mA), higher frequency ripple may be reduced by using larger output capacitors.
2. A feedforward capacitor across the resistor divider used with the adjustable part is effective in reducing ripple only for output voltages greater than 5V and only for frequencies less than 100kHz.
3. Input-to-output voltage differential has little effect on ripple rejection until the regulator actually enters a dropout condition of 0.2V to 0.6V.

If ripple rejection needs to be improved, an input filter can be added. This filter can be a simple RC filter using a 1Ω to 10Ω resistor. A 3.3Ω resistor for instance, combined with a 0.3Ω ESR solid tantalum capacitor, will give an additional 20dB ripple rejection. The size of the resistor will be dictated by maximum load current. If the maximum voltage drop allowable across the resistor is "V_R," and maximum load current is I_{LOAD}, $R = V_R/I_{LOAD}$. At light loads, larger resistors and smaller capacitors can be used to save space. At heavier loads an inductor may have to be used in place of the resistor. The value of the inductor can be calculated from:

$$L_{FIL} = \frac{ESR}{2\pi(f)\left(10^{rr/20}\right)}$$

ESR = Effective series resistance of filter capacitor. This assumes that the capacitive reactance is small compared to ESR, a reasonable assumption for solid tantalum capacitors above 2.2µF and 50kHz.

f = Ripple frequency

rr = Ripple rejection ratio of filter in dB

Example: ESR = 1.2Ω, f = 100kHz, rr = –25dB.

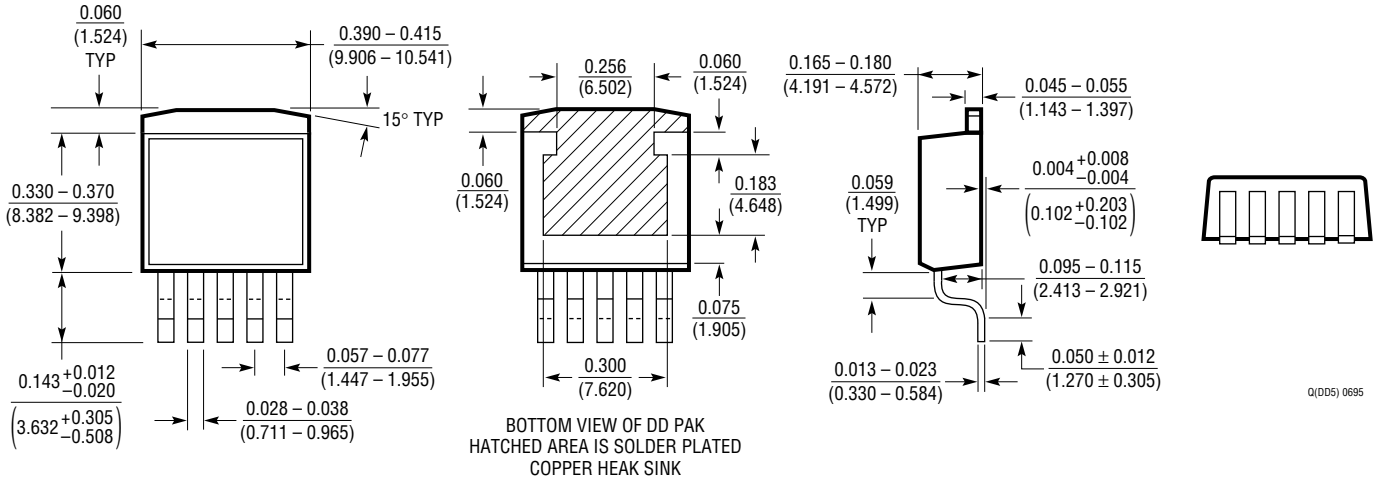
$$L_{FIL} = \frac{1.2}{6.3\left(10^{5}\right)\left(10^{-25/20}\right)} = 34\mu H$$

Solid tantalum capacitors are suggested for the filter to keep filter Q fairly low. This prevents unwanted ringing at the resonant frequency of the filter and oscillation problems with the filter/regulator combination.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

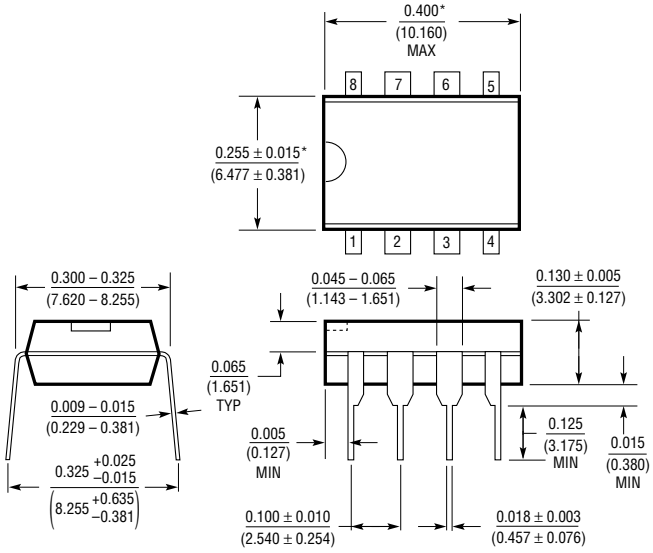
Q Package
5-Lead Plastic DD Pak
(LTC DWG # 05-08-1461)



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

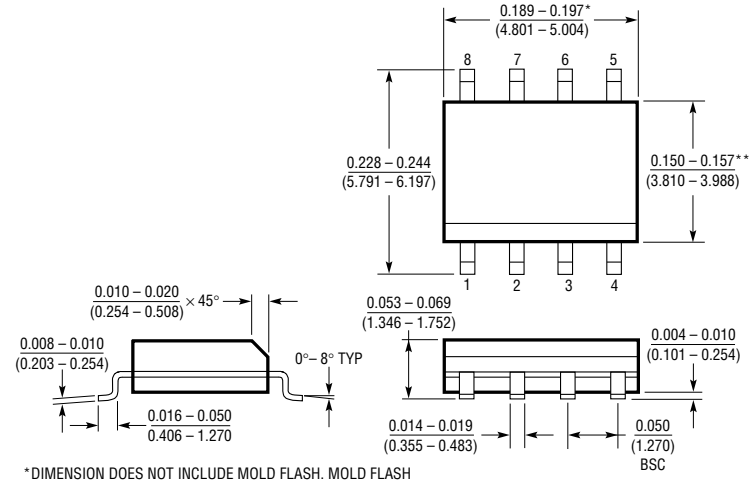
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N8 0695

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

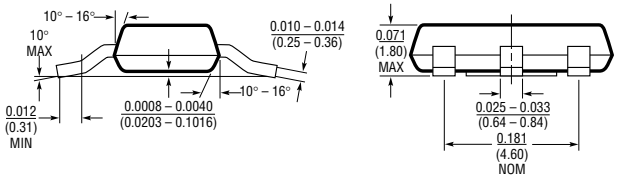


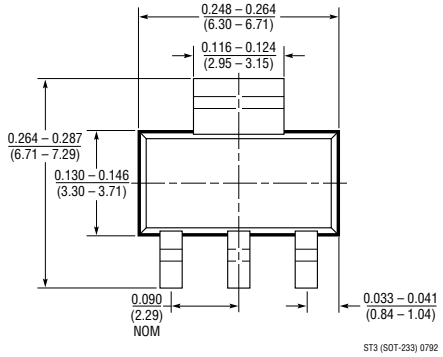
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0695

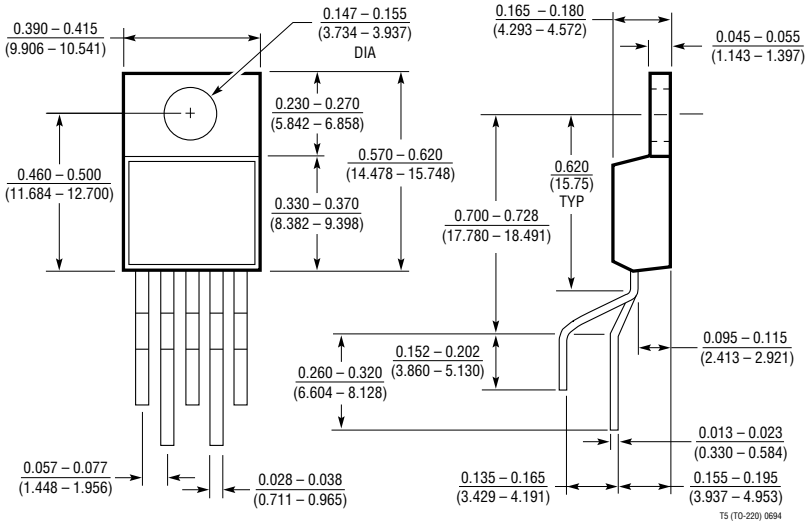
ST Package
3-Lead Plastic SOT-223
(LTC DWG # 05-08-1630)





ST3 (SOT-233) 0792

T Package
5-Lead Plastic TO-220 (Standard)
(LTC DWG # 05-08-1421)



T5 (TO-220) 0694

RELATED PARTS

LT1121	150mA Positive Micropower Low Dropout Regulator with Shutdown
LT1129	700mA Positive Micropower Low Dropout Regulator with Shutdown
LT1185	3A Negative Low Dropout Regulator
LT1521	300mA Positive Micropower Low Dropout Regulator with Shutdown
LT1529	3A Positive Micropower Low Dropout Regulator with Shutdown

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LT/GP 0996 5K REV B • PRINTED IN USA

National Semiconductor

January 1995

LM137/LM337
3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM337 are ideal complements to the LM117/LM317 adjustable positive regulators.

Features

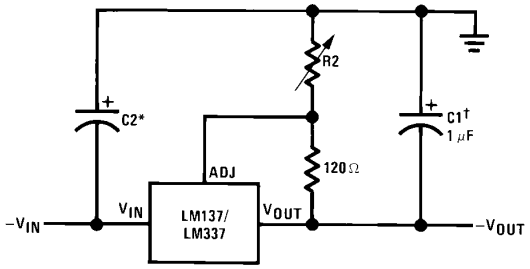
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- P+ Product Enhancement tested
- Standard 3-lead transistor package
- Output is short circuit protected

LM137 Series Packages and Power Capability

Device	Package	Rated Power Dissipation	Design Load Current
LM137/337	TO-3 (K) TO-39 (H)	20W 2W	1.5A 0.5A
LM337	TO-220 (T)	15W	1.5A

Typical Applications

Adjustable Negative Voltage Regulator



TL/H/9067–1

Full output current not available at high input-output voltages

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4″ from power-supply filter capacitor

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operating Junction Temperature Range	
LM137	−55°C to +150°C
LM337	0°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Plastic Package (Soldering, 4 sec.)	260°C
ESD Rating	2k Volts

Electrical Characteristics (Note 1)

Parameter	Conditions	LM137			LM337			Units
		Min	Typ	Max	Min	Typ	Max	
Line Regulation	$T_j = 25°C$, $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$ (Note 2) $I_L = 10$ mA		0.01	0.02		0.01	0.04	%/V
Load Regulation	$T_j = 25°C$, $10\text{ mA} \le I_{OUT} \le I_{MAX}$		0.3	0.5		0.3	1.0	%
Thermal Regulation	$T_j = 25°C$, 10 ms Pulse		0.002	0.02		0.003	0.04	%/W
Adjustment Pin Current			65	100		65	100	μA
Adjustment Pin Current Change	$10\text{ mA} \le I_L \le I_{MAX}$ $3.0V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, $T_A = 25°C$		2	5		2	5	μA
Reference Voltage	$T_j = 25°C$ (Note 3) $3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 3) $10\text{ mA} \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	−1.225 −1.200	−1.250 −1.250	−1.275 −1.300	−1.213 −1.200	−1.250 −1.250	−1.287 −1.300	V V
Line Regulation	$3V \le \lvert V_{IN} - V_{OUT} \rvert \le 40V$, (Note 2)		0.02	0.05		0.02	0.07	%/V
Load Regulation	$10\text{ mA} \le I_{OUT} \le I_{MAX}$, (Note 2)		0.3	1		0.3	1.5	%
Temperature Stability	$T_{MIN} \le T_j \le T_{MAX}$		0.6			0.6		%
Minimum Load Current	$\lvert V_{IN} - V_{OUT} \rvert \le 40V$ $\lvert V_{IN} - V_{OUT} \rvert \le 10V$		2.5 1.2	5 3		2.5 1.5	10 6	mA mA
Current Limit	$\lvert V_{IN} - V_{OUT} \rvert \le 15V$ K and T Package H Package $\lvert V_{IN} - V_{OUT} \rvert = 40V$, $T_j = 25°C$ K and T Package H Package	1.5 0.5 0.24 0.15	2.2 0.8 0.4 0.17	3.5 1.8	1.5 0.5 0.15 0.10	2.2 0.8 0.4 0.17	3.7 1.9	 A A A A
RMS Output Noise, % of V_{OUT}	$T_j = 25°C$, $10\text{ Hz} \le f \le 10\text{ kHz}$		0.003			0.003		%
Ripple Rejection Ratio	$V_{OUT} = -10V$, f = 120 Hz $C_{ADJ} = 10\ \mu F$	 66	60 77		 66	60 77		dB dB
Long-Term Stability	$T_j = 125°C$, 1000 Hours		0.3	1		0.3	1	%
Thermal Resistance, Junction to Case	H Package K Package T Package		12 2.3	15 3		12 2.3 4	15 3	°C/W °C/W °C/W
Thermal Resistance, Junction to Ambient (No Heat Sink)	H Package K Package T Package		140 35			140 35 50		°C/W °C/W °C/W

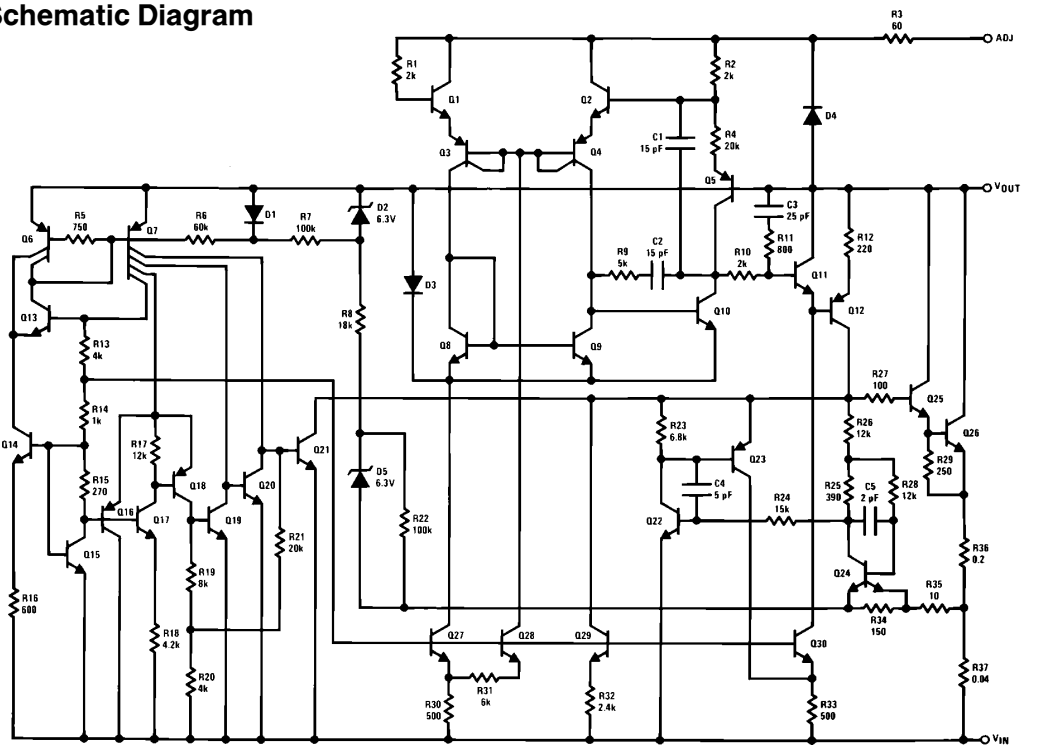
Note 1: Unless otherwise specified, these specifications apply $-55°C \le T_j \le +150°C$ for the LM137, $0°C \le T_j \le +125°C$ for the LM337; $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 package and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39 and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages, and 0.2A for the TO-39 package.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point ⅛″ below the base of the TO-3 and TO-39 packages.

Note 3: Selected devices with tightened tolerance reference voltage available.

Note 4: Refer to RETS137H drawing for LM137H or RETS137K drawing for LM137K military specifications.

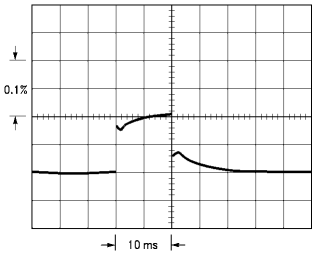
Schematic Diagram



TL/H/9067–2

Thermal Regulation

When power is dissipated in an IC, a temperature gradient occurs across the IC chip affecting the individual IC circuit components. With an IC regulator, this gradient can be especially severe since power dissipation is large. Thermal regulation is the effect of these temperature gradients on output voltage (in percentage output change) per Watt of power change in a specified time. Thermal regulation error is independent of electrical regulation or temperature coefficient, and occurs within 5 ms to 50 ms after a change in power dissipation. Thermal regulation depends on IC layout as well as electrical design. The thermal regulation of a voltage regulator is defined as the percentage change of V_{OUT}, per Watt, within the first 10 ms after a step of power is applied. The LM137's specification is 0.02%/W, max.

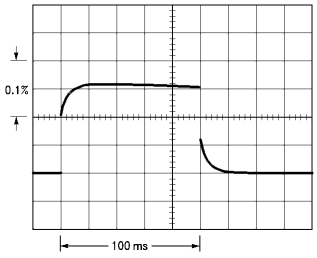


TL/H/9067–3

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_{IL} = 0A \rightarrow 0.25A \rightarrow 0A$
Vertical sensitivity, 5 mV/div

FIGURE 1

In *Figure 1*, a typical LM137's output drifts only 3 mV (or 0.03% of $V_{OUT} = -10V$) when a 10W pulse is applied for 10 ms. This performance is thus well inside the specification limit of 0.02%/W × 10W = 0.2% max. When the 10W pulse is ended, the thermal regulation again shows a 3 mV step at the LM137 chip cools off. Note that the load regulation error of about 8 mV (0.08%) is additional to the thermal regulation error. In *Figure 2*, when the 10W pulse is applied for 100 ms, the output drifts only slightly beyond the drift in the first 10 ms, and the thermal error stays well within 0.1% (10 mV).



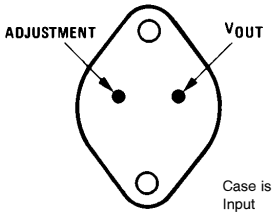
TL/H/9067–4

LM137, $V_{OUT} = -10V$
$V_{IN} - V_{OUT} = -40V$
$I_L = 0A \rightarrow 0.25A \rightarrow 0A$
Horizontal sensitivity, 20 ms/div

FIGURE 2

Connection Diagrams

TO-3
Metal Can Package

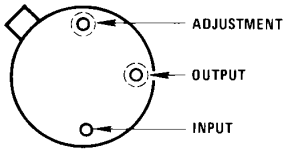


TL/H/9067–5

Bottom View
Order Number LM137K/883
See NS Package Number K02C

Order Number LM337K STEEL
See NS Package Number K02A

TO-39
Metal Can Package

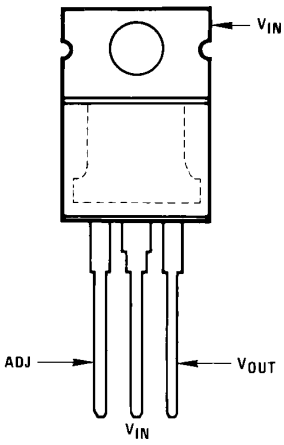


TL/H/9067–6

Bottom View

Order Number LM137H, LM137H/883 or LM337H
See NS Package Number H03A

TO-220
Plastic Package



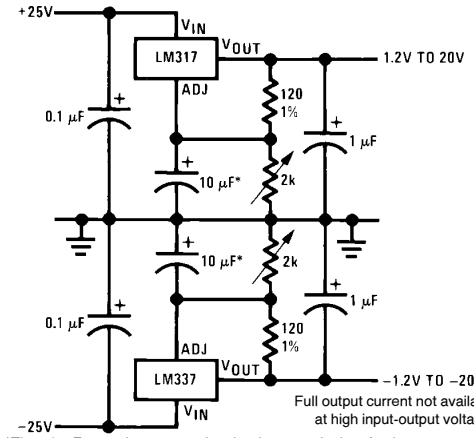
TL/H/9067–7

Front View

Order Number LM337T
See NS Package Number T03B

Typical Applications (Continued)

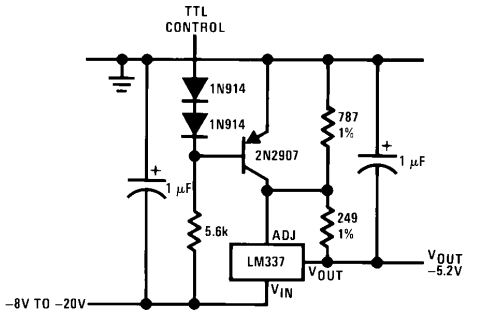
Adjustable Lab Voltage Regulator



*The 10 μF capacitors are optional to improve ripple rejection

TL/H/9067–9

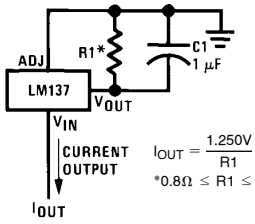
−5.2V Regulator with Electronic Shutdown*



TL/H/9067–10

*Minimum output ≅ −1.3V when control input is low

Current Regulator

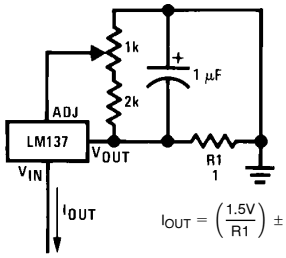


$I_{OUT} = \frac{1.250V}{R1}$

*0.8Ω ≤ R1 ≤ 120Ω

TL/H/9067–11

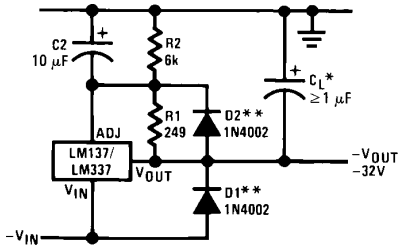
Adjustable Current Regulator



$I_{OUT} = \left(\frac{1.5V}{R1}\right) \pm 15\%$ adjustable

TL/H/9067–12

Negative Regulator with Protection Diodes

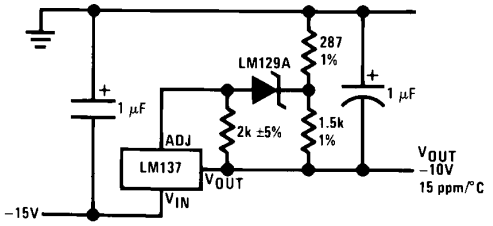


TL/H/9067–13

*When C_L is larger than 20 μF, D1 protects the LM137 in case the input supply is shorted

**When C2 is larger than 10 μF and $-V_{OUT}$ is larger than −25V, D2 protects the LM137 in case the output is shorted

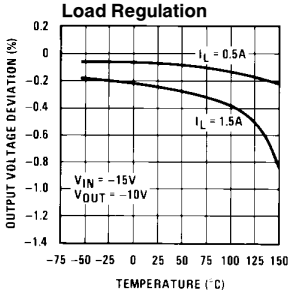
High Stability −10V Regulator



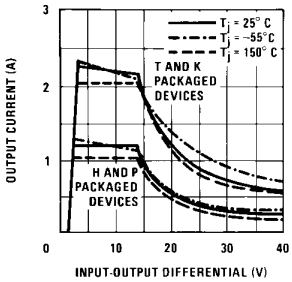
TL/H/9067–14

Typical Performance Characteristics (K Steel and T Packages)

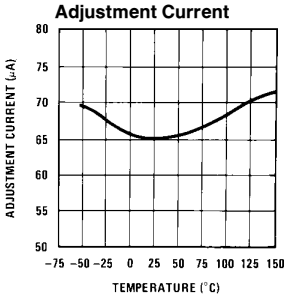
Load Regulation



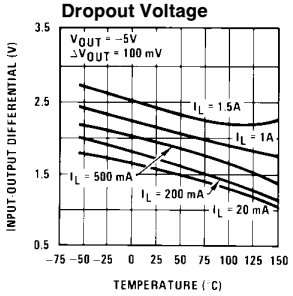
Current Limit



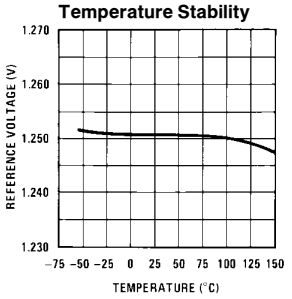
Adjustment Current



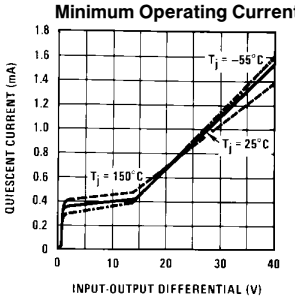
Dropout Voltage



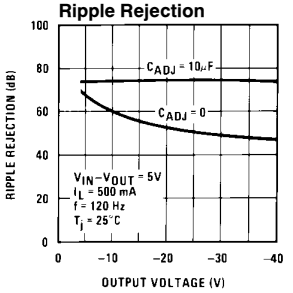
Temperature Stability



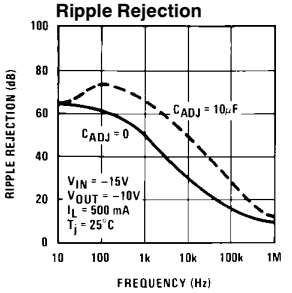
Minimum Operating Current



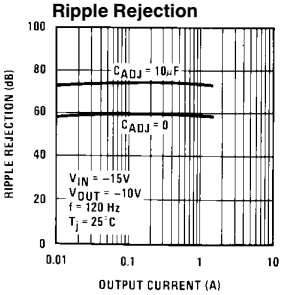
Ripple Rejection



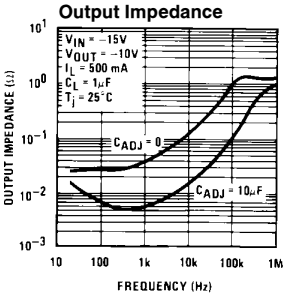
Ripple Rejection



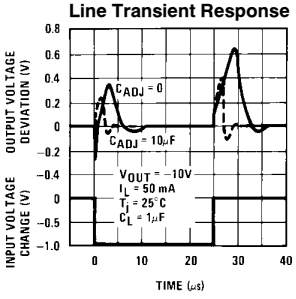
Ripple Rejection



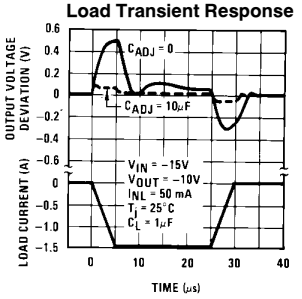
Output Impedance



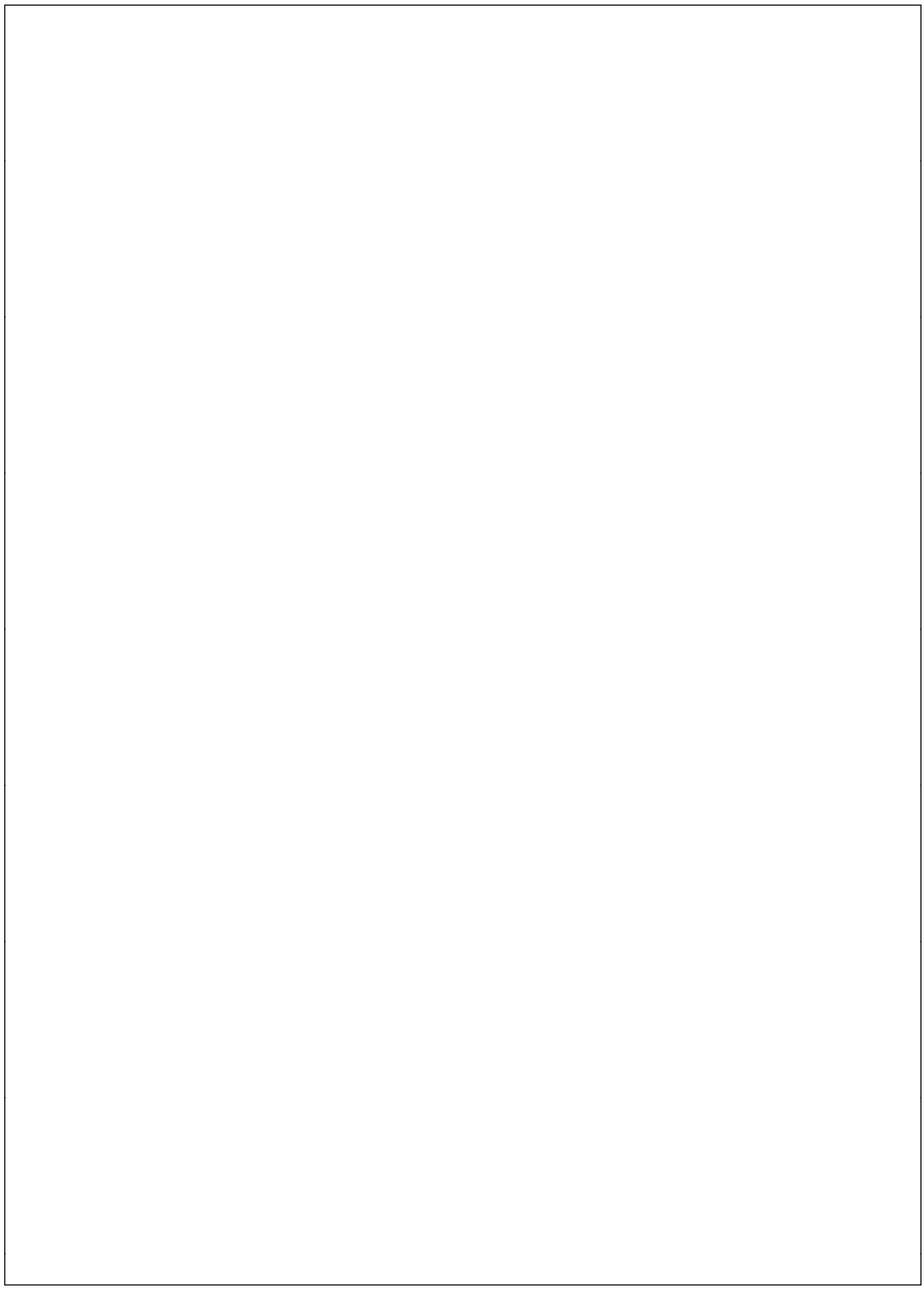
Line Transient Response



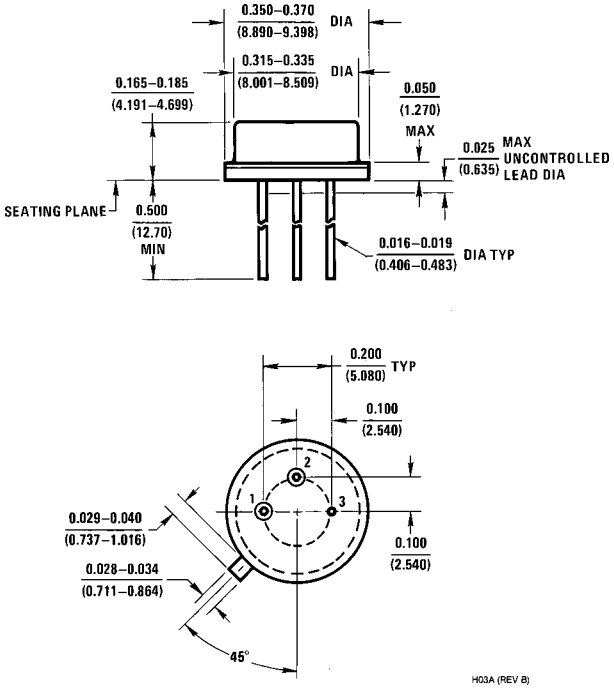
Load Transient Response



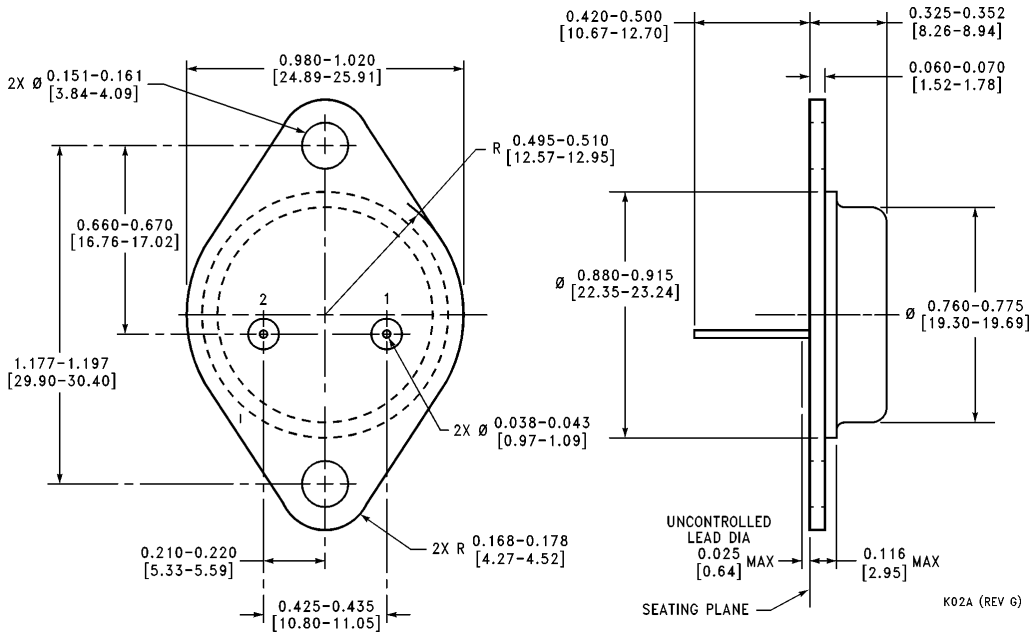
TL/H/9067–15



Physical Dimensions inches (millimeters)

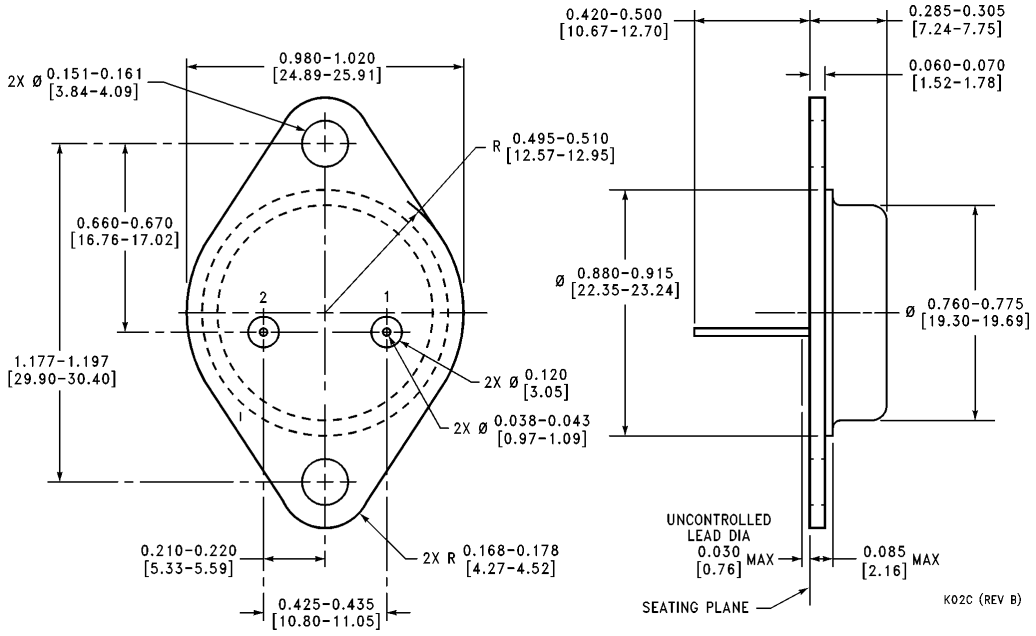


Metal Can Package (H)
Order Number LM137H, LM137H/883 or LM337H
NS Package Number H03A



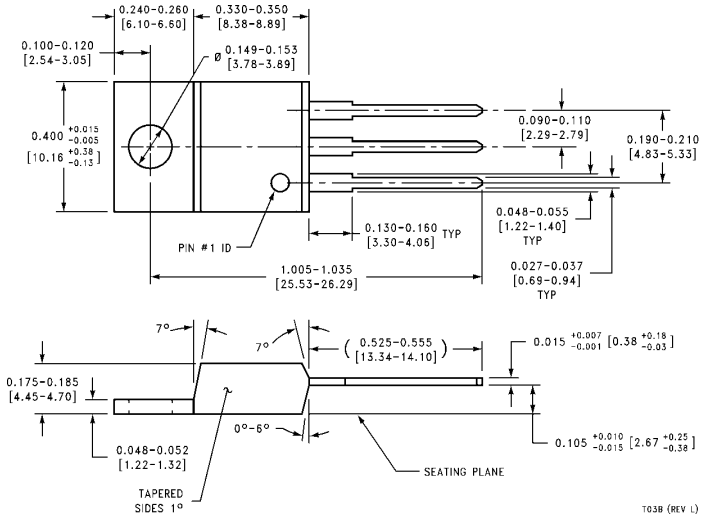
Metal Can Package (K)
Order Number LM337K STEEL
NS Package Number K02A

Physical Dimensions inches (millimeters) (Continued)



Mil-Aero Metal Can Package (K)
Order Number LM137K/883
NS Package Number K02C

Physical Dimensions inches (millimeters) (Continued)



TO-220 Plastic Package (T)
Order Number LM337T
NS Package Number T03B

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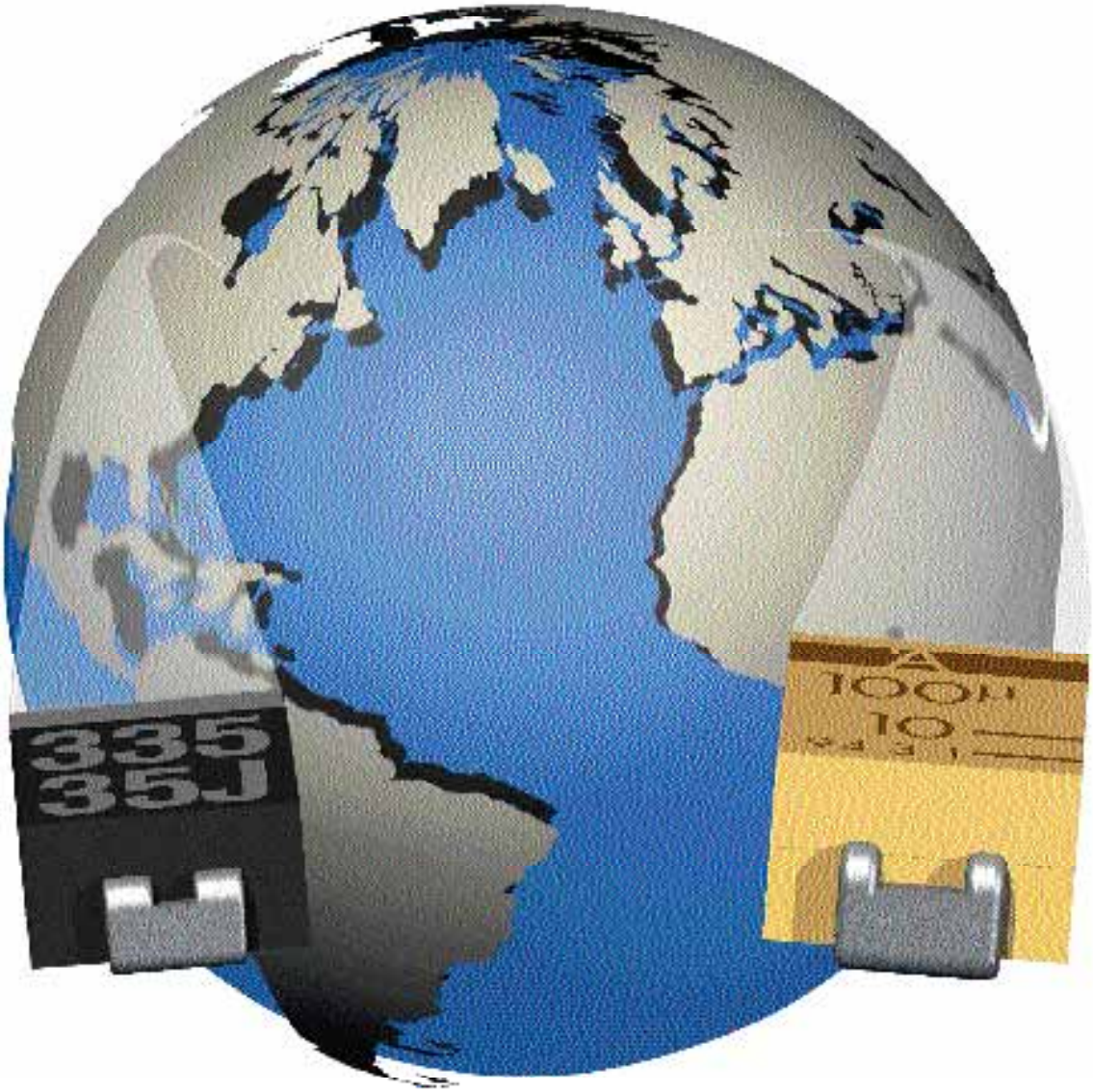


Surface Mount Tantalum Capacitors

Foreword

AVX offers a broad line of molded solid tantalum capacitors in a wide range of sizes, styles, and ratings to meet your design needs. This catalog combines into one source AVX's SMD tantalum capacitor information from its worldwide tantalum operations.

The TAJ series includes EIA standard case sizes and ratings, along with extended range values. Low profile packages and EIAJ standard case sizes, MIL-Style CWR11 components are available as part of the TAJ family.

The TPS Low ESR SMD product line was introduced last year and is included in this catalog to provide a comprehensive listing of our tantalum surface mount lines. TPS has its own catalog which covers performance and applications in depth. This catalog may be obtained from your local AVX representative.

The TAZ Series offers high volume efficiency components in a wide variety of footprints. Five of those footprints have a nominal height of 0.050 inches which make them ideal for low profile applications.

The TAZ series is qualified as the MIL-Style CWR09, the molded equivalent of the MIL-Style CWR06. Two new case sizes are added to this series, increasing the capacitance/voltage ratings available for both low and high values. Extended range values are also available in all series.

AVX offers tantalum applications service for use by our customers, please contact your local representative if you wish to discuss any special requirements.

AVX has become a world leader in tantalum capacitor technology and is continuing to make significant investments in equipment and research to maintain that leadership.

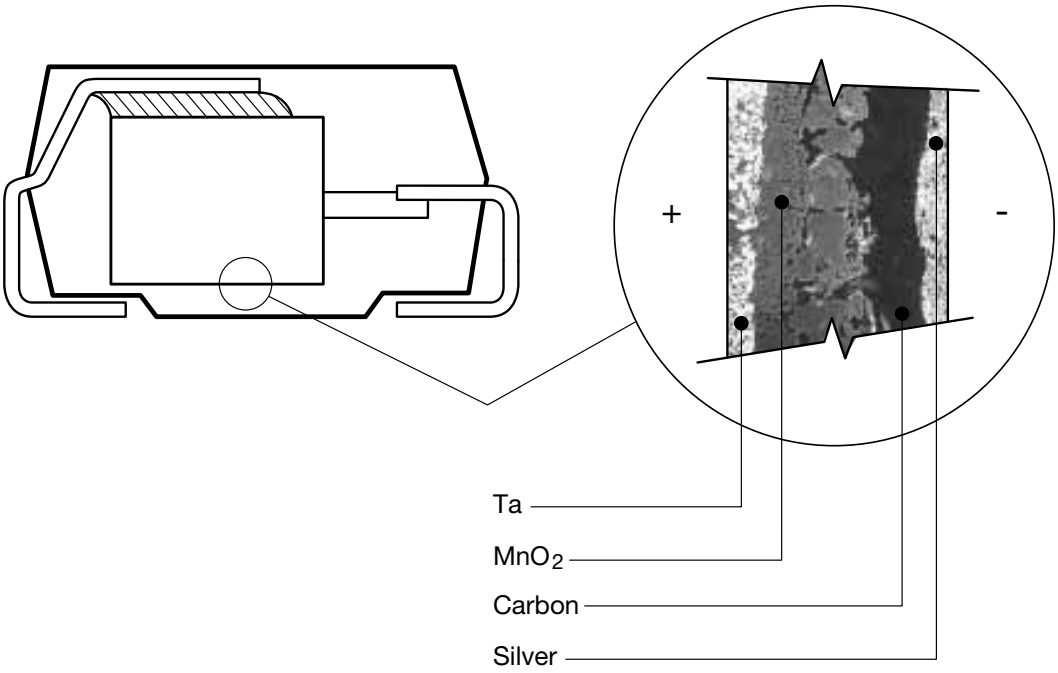
Contents

Surface Mount Tantalum Capacitors

Technical Summary and Application Guidelines

Section 1 – TAJ, TAZ, and TPS

The AVX series of molded tantalum chips are designed for surface mount applications and are equally suitable for hybrid applications. They are available tape and reel packaged for high volume automatic assembly techniques.



Design and Application Features

1. Flat top surface for high speed pick-up — compatible with high speed automatic onsertion equipment.

2. Regular molded shape — allows accurate transfer and placement during onsertion.

3. Glue pads on underside of TAJ/TPS ranges permit consistent, strong bonding to circuit board prior to soldering.

4. Consistent termination dimensions — allows reliable pad design and a consistent “fit” — helps to eliminate “tombstoning” effects and reduces rotational effects.

5. Compliant terminations — transfer of thermo-mechanical stresses during operation and mechanical stresses during equipment servicing to the component are reduced.

6. Rugged construction helps to prevent damage during mounting and to ensure compatibility with all systems for soldering (infra-red, wave solder, reflow solder, vapor phase) and conductive epoxy resin mounting techniques.

7. Resistant to flux removal solvents including Aqueous systems used with vapor phase soldering.

8. All parts are coded on uppermost surface with videcon-readable polarity marking, cap value, and voltage.

9. High density packaging on 8 and 12 mm blister tape, available on 7" and 13" reels.

10. Qualified to IECQ, CECC and MIL specifications, TAJ/TPS in compliance with EIA standards.

11. New low profile case sizes including the new “R” case compatible with “0805” footprint. Maximum height for low profile is 1.2mm (0.047").

Surface Mount Tantalum Capacitors

TAJ Series — Solid Tantalum Chip Capacitors (EIA Standard)

The TAJ standard series encompasses the four key sizes recognized by major OEMs throughout the world, together with the new high profile E case (7343H size) and two cases conforming to the EIA-J standard.

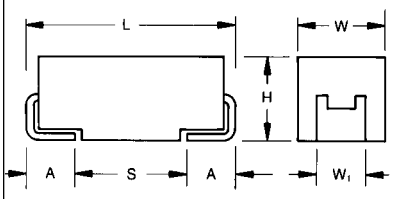
Available with standard capacitance tolerances of ±10% and ±20%.

Operational temperature -55°C to +85°C at rated voltage and up to +125°C with voltage derating in applications utilizing recommended series resistance.

TAJ is available in standard and extended ranges.

Note on sizes: A, B, C, D - EIA standard EIA-535BAAC
E - Extended range (high profile D case, 7343H EIA-535BAAC)
M, N - EIA-J standard

For CWR11 ratings see pages 19 - 21.



Case Dimensions millimeters (inches)

Code	EIA Code	W+0.2 (0.008) -0.1 (0.004)	L± 0.2 (0.008)	H+0.2 (0.008) - 0.1 (0.004)	W_1±0.2 (0.008)	A+ 0.3 (0.012) - 0.2 (0.008)	S Min.
A	3216	1.6 (0.063)	3.2 (0.126)	1.6 (0.063)	1.2 (0.047)	0.8 (0.031)	1.1 (0.043)
B	3528	2.8 (0.110)	3.5 (0.138)	1.9 (0.075)	2.2 (0.087)	0.8 (0.031)	1.4 (0.055)
C	6032	3.2 (0.126)	6.0 (0.236)	2.6 (0.102)	2.2 (0.087)	1.3 (0.051)	2.9 (0.114)
D	7343	4.3 (0.169)	7.3 (0.287)	2.9 (0.114)	2.4 (0.094)	1.3 (0.051)	4.4 (0.173)
E	7343H	4.3 (0.169)	7.3 (0.287)	4.1 (0.162)	2.4 (0.094)	1.3 (0.051)	4.4 (0.173)
M	4726*	2.6 (0.102)	4.7 (0.185)	2.1 (0.083)	1.4 (0.055)	0.8 (0.031)	2.7 (0.106)
N	5846*	4.6 (0.181)	5.8 (0.228)	3.2 (0.126)	2.4 (0.094)	1.3 (0.051)	2.8 (0.110)

W_1 dimension applies to the termination width for A dimensional area only.
*EIA-J Case Reference

How to Order: TAJ C 106 M 025 R **

Type

Case Code (See table above)

Capacitance Code
pF code: 1st two digits represent significant figures, 3rd digit represents multiplier (number of zeros to follow)

Tolerance
K=±10%, M=±20%, (J=±5%, consult your AVX representative for details)

Rated DC Voltage

Packaging/Leadframe Finish (Consult page 10 for details)

Additional characters may be added for special requirements

Technical Data:		All technical data relate to an ambient temperature of +25°C							
Capacitance Range:		0.1 µF to 330 µF							
Capacitance Tolerance:		±20%; ±10%							
Rated Voltage DC (V_R)	≦+85°C:	4	6.3	10	16	20	25	35	50
Category Voltage (V_C)	+125°C:	2.7	4	7	10	13	17	23	33
Surge Voltage (V_S)	≦+85°C:	5.2	8	13	20	26	32	46	65
	+125°C:	3.2	5	8	12	16	20	28	40
Temperature Range:		-55°C to +125°C							
Environmental Classification:		55/125/56 (IEC 68-2)							
Dissipation Factor:		≦0.04 for C_R ≦1.0 µF							
		≦0.06 for C_R >1.0 µF							
		≦0.08 for E case with C_R ≧100 µF							

TAJ Series — Solid Tantalum Chip Capacitors (EIA Standard)

Standard Range (EIA and EIA-J sizes). See below for extended range.

Capacitance Range (letter denotes case code)															
Capacitance		Rated voltage DC (V_R) at 85°C													
µF	Code	4V		6.3V		10V		16V		20V		25V		35V		50V	
		Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.	Std.	Alt.
0.1	104													A		A	
0.15	154													A		B	
0.22	224													A		B	
0.33	334													A		B	
0.47	474											A		B	M	C	
0.68	684									A		A		B	M	C	
1.0	105							A		A				B	M	C	
1.5	155					A		A				B	M	C		D	
2.2	225			A		A		B	M	B	M			C		D	
3.3	335	A		A				B	M	B	M	C		C		D	
4.7	475	A				B	M	B	M	C		C		D		D	
6.8	685			B	M	B	M	C		C		D		D	N		
10	106	B	M	B	M	C		C				D	N	D	N		
15	156	B	M	C		C				D		D	N				
22	226	C		C				D		D	N						
33	336	C				D		D	N								
47	476	D		D	N	D	N										
68	686	D		D	N												
100	107	D	N														

"Std" denotes EIA standard sizes
"Alt" denotes EIA J sizes

Extended Range/Developmental Range

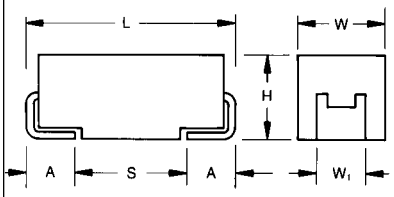
Capacitance Range (letter denotes case code)								
Capacitance		Rated voltage DC (V_R) at 85°C						
µF	Code	4V	6.3V	10V	16V	20V	25V	35V	50V
0.1	104								
0.15	154								A
0.22	224								A
0.33	334								
0.47	474							A	
0.68	684							A	
1.0	105						A	A	
1.5	155					A	A	B M	
2.2	225				A		B	B M	
3.3	335			A	A		B	B	
4.7	475		A	A	A	A/B	B	C	
6.8	685	A	A	A	A/B		C	C	D
10	106	A	A	A/B	B M	B/C	C		
15	156	A	A/B	B	B/C	C		D	
22	226	A/B	B	B/C M	C	C	D	E	
33	336	B	B/C	C	C	D	E		
47	476	B/C M	C	C	D	D E			
68	686	C	C	D	D	E			
100	107	C	D	D	E				
150	157	D	D	D/E	E				
220	227	D	E	E					
330	337	E	E						

Ratings outside this matrix may be available upon request.
Please contact your AVX representative for availability of developmental range.

Surface Mount Tantalum Capacitors

TAJ Series — Low Profile Solid Tantalum Chip Capacitors (EIA Standard)

Three additional case sizes are available in the TAJ range offering ultra low profile solid tantalum chip capacitors. Designed for applications where maximum height of components above or below board are of prime consideration, this height of 1.2mm equates to that of a standard integrated circuit package after mounting. Also available is the ultra compact 0805 equivalent in a fully molded package. The S&T footprints are identical to the A&B case size parts.



Case Dimensions millimeters (inches—Metric Dimensions Govern)

Code	EIA Code	W+0.2 (0.008) - 0.1 (0.004)	L±0.2 (0.008)	H max.	W_1±0.1 (0.004)	A+ 0.3 (0.012) - 0.1 (.004)	S Min.
0805 Equivalent							
R	2012	1.3 (0.05)	2.05 (0.08)	1.2 (0.047)	1.2 (0.047)	0.5 (0.020)	0.85 (0.033)
Low Profile Versions of A & B Case							
S	3216L	1.6 (0.06)	3.2 (0.12)	1.2 (0.047)	1.2 (0.047)	0.8 (0.031)	1.1 (0.043)
T	3528L	2.8 (0.11)	3.5 (0.14)	1.2 (0.047)	2.2 (0.087)	0.8 (0.031)	1.4 (0.055)

W_1 dimension applies to the termination width for A dimensional area only.
Pad Stand-off is 0.1±0.1.

Capacitance and Voltage Range (letter denotes case code)/Developmental Range

Capacitance		Rated voltage DC (V_R) at 85°C					
µF	Code	2V	4V	6.3V	10V	16V	20V
0.1	104						R/S
0.15	154						R/S
0.22	224						R/S
0.33	334						R/S
0.47	474						R/S
0.68	684					R/S	R/S/T
1.0	105				R/S	R/S	R/S/T
1.5	155			R/S	R/S	S	T
2.2	225		R/S	R/S	S	T	T
3.3	335		R/S	R/S	T	T	
4.7	475	R	R/S	S/T	T		
6.8	685	R	S/T	T			
10	106	S	T		T		

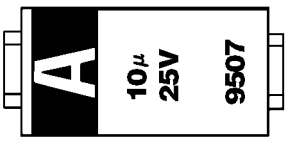
Please contact your AVX representative for availability of Developmental Range.

Marking: TAJ Series

For TAJ, the positive end of body has videcon readable polarity bar marking, with the AVX logo "A" as shown in the diagram. Bodies are marked by indelible laser marking on top surface with capacitance value, voltage and date of manufacture. Due to the small size of the A, B, M, R, S and T cases, a voltage code is used as shown below:

Voltage Code A, B, S and T Cases	Rated Voltage at 85°C
G	4
J	6.3
A	10
C	16
D	20
E	25
V	35
T	50

A, B, M, R, S and T Case:
1. Voltage Code (see table)
2. Capacitance in µF
3. Date Code



C, D, E and N Case:
1. Capacitance in µF
2. Rated Voltage at 85°C
3. Date Code

Polarity bar indicates anode (+) termination

Ratings and Part Number Reference

AVX Part No.	Case Size	Capacitance µF	DCL (µA) Max.	DF % Max.	ESR max. (Ω) @ 100 kHz
4 volt @ 85°C (2.5 volt @ 125°C)					
TAJA335(*)004	A	3.3	0.5	6	9.0
TAJA475(*)004	A	4.7	0.5	6	7.5
TAJA685(*)004	A	6.8	0.5	6	6.5
TAJA106(*)004	A	10	0.5	6	6.0
TAJB106(*)004	B	10	0.5	6	4.0
TAJM106(*)004	M	10	0.5	6	4.5
TAJA156(*)004	A	15	0.6	6	4.0
TAJB156(*)004	B	15	0.6	6	3.0
TAJM156(*)004	M	15	0.6	6	3.5
TAJA226(*)004	A	22	0.9	6	3.5
TAJB226(*)004	B	22	0.9	6	2.5
TAJC226(*)004	C	22	1.4	6	2.3
TAJB336(*)004	B	33	1.4	6	2.8
TAJC336(*)004	C	33	1.9	6	2.0
TAJB476(*)004	B	47	1.9	6	2.4
TAJC476(*)004	C	47	1.9	6	1.8
TAJD476(*)004	D	47	1.9	6	1.8
TAJC686(*)004	C	68	2.7	6	1.6
TAJD686(*)004	D	68	2.7	6	1.1
TAJC107(*)004	C	100	4.0	6	1.3
TAJD107(*)004	D	100	4.0	6	0.9
TAJN107(*)004	N	100	4.0	6	1.5
TAJD157(*)004	D	150	6.0	6	0.9
TAJE227(*)004	E	220	8.8	8	0.9
TAJE337(*)004	E	330	13.2	8	0.9
6.3 volt @ 85°C (4 volt @ 125°C)					
TAJA225(*)006	A	2.2	0.5	6	9.0
TAJA335(*)006	A	3.3	0.5	6	7.0
TAJA475(*)006	A	4.7	0.5	6	6.0
TAJA685(*)006	A	6.8	0.5	6	5.0
TAJB685(*)006	B	6.8	0.5	6	4.0
TAJM685(*)006	M	6.8	0.5	6	4.5
TAJA106(*)006	A	10	0.6	6	4.0
TAJB106(*)006	B	10	0.6	6	3.0
TAJM106(*)006	M	10	0.6	6	3.5
TAJA156(*)006	A	15	1.0	6	3.5
TAJB156(*)006	B	15	1.0	6	2.5
TAJC156(*)006	C	15	1.0	6	2.5
TAJM156(*)006	M	15	1.0	6	3.5
TAJB226(*)006	B	22	1.4	6	2.5
TAJC226(*)006	C	22	1.4	6	2.0
TAJB336(*)006	B	33	2.1	6	2.2
TAJC336(*)006	C	33	2.1	6	1.8
TAJC476(*)006	C	47	3.0	6	1.6
TAJD476(*)006	D	47	3.0	6	1.1
TAJC686(*)006	C	68	4.3	6	1.6
TAJD686(*)006	D	68	4.3	6	0.9
TAJD107(*)006	D	100	6.3	6	0.9
TAJD157(*)006	D	150	9.0	6	0.9
TAJE227(*)006	E	220	13.2	8	0.9
TAJE337(*)006	E	330	19.8	8	0.9

AVX Part No.	Case Size	Capacitance µF	DCL (µA) Max.	DF % Max.	ESR max. (Ω) @ 100 kHz
10 volt @ 85°C (6.3 volt @ 125°C)					
TAJA155(*)010	A	1.5	0.5	6	10.0
TAJA225(*)010	A	2.2	0.5	6	7.0
TAJA335(*)010	A	3.3	0.5	6	5.5
TAJA475(*)010	A	4.7	0.5	6	5.0
TAJB475(*)010	B	4.7	0.5	6	4.0
TAJM475(*)010	M	4.7	0.5	6	4.5
TAJA685(*)010	A	6.8	0.7	6	4.0
TAJB685(*)010	B	6.8	0.7	6	3.0
TAJM685(*)010	M	6.8	0.7	6	3.5
TAJA106(*)010	A	10	1.0	6	3.0
TAJB106(*)010	B	10	1.0	6	2.5
TAJM106(*)010	M	10	1.0	6	3.5
TAJC106(*)010	C	10	1.0	6	2.5
TAJB156(*)010	B	15	1.6	6	2.8
TAJC156(*)010	C	15	1.5	6	2.0
TAJB226(*)010	B	22	2.2	6	2.4
TAJC226(*)010	C	22	2.2	6	1.8
TAJC336(*)010	C	33	3.3	6	1.6
TAJD336(*)010	D	33	3.3	6	1.1
TAJC476(*)010	C	47	4.7	6	1.2
TAJD476(*)010	D	47	4.7	6	0.9
TAJN476(*)010	N	47	4.7	6	1.5
TAJD686(*)010	D	68	6.8	6	0.9
TAJD107(*)010	D	100	10.0	6	0.9
TAJE157(*)010	E	150	15.0	6	0.9
TAJE227(*)010	E	220	22.0	8	0.9
16 volt @ 85°C (10 volt @ 125°C)					
TAJA105(*)016	A	1.0	0.5	4	11.0
TAJA155(*)016	A	1.5	0.5	6	8.0
TAJA225(*)016	A	2.2	0.5	6	6.5
TAJB225(*)016	B	2.2	0.5	6	5.5
TAJM225(*)016	M	2.2	0.5	6	6.5
TAJA335(*)016	A	3.3	0.5	6	5.0
TAJB335(*)016	B	3.3	0.5	6	4.5
TAJM335(*)016	M	3.3	0.5	6	5.0
TAJA475(*)016	A	4.7	0.8	6	4.0
TAJB475(*)016	B	4.7	0.8	6	3.5
TAJM475(*)016	M	4.7	0.8	6	3.5
TAJB685(*)016	B	6.8	1.1	6	2.5
TAJC685(*)016	C	6.8	1.1	6	2.5
TAJB106(*)016	B	10	1.6	6	2.8
TAJM106(*)016	M	10	1.6	6	2.8
TAJC106(*)016	C	10	1.6	6	2.0
TAJB156(*)016	B	15	2.4	6	2.5
TAJC156(*)016	C	15	2.4	6	1.8
TAJC226(*)016	C	22	3.5	6	1.6
TAJD226(*)016	D	22	3.5	6	1.1
TAJD336(*)016	D	33	5.3	6	0.9
TAJN336(*)016	N	33	5.3	6	1.5
TAJD476(*)016	D	47	7.5	6	0.9
TAJD686(*)016	D	68	10.8	6	0.9
TAJE107(*)016	E	100	16.0	6	0.9

For 10% tolerance, insert 'K' in (*) above.
For 20% tolerance, insert 'M' in (*) above. (K tolerance may be supplied in lieu of M tolerance.)
NOTE: Voltage ratings are minimum values. We reserve the right to supply higher voltage ratings in the same case size, to the same reliability standards.

CHIP EMIFIL®

muRata

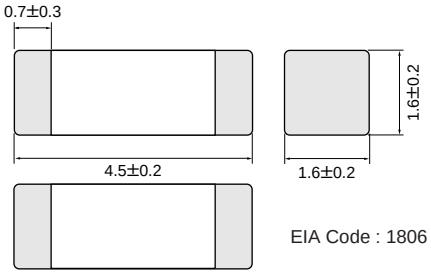
Chip Ferrite Bead Inductor BLM41 Series

■SPECIFICATIONS

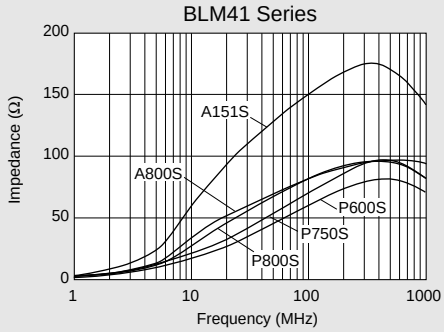
Part Number	Impedance (Ω) (Typ.) at 100MHz	Rated Current (mA)	DC Resistance (Ω max.)	Operating Temp. Range (°C)
BLM41P600S	60	6000*	0.01	−55 to +125
BLM41P750S	75	3000*	0.025	
BLM41P800S	80	1000*	0.10	
BLM41A800S	80	500		
BLM41A151S	150	200	0.50	

✻ BLM41P series : Please derate the maximum current, as shown in previous page, for temperatures above +85°C.

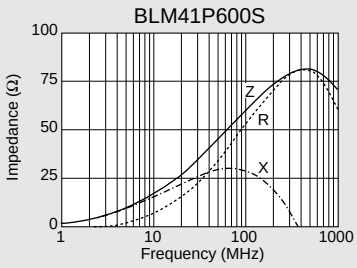
■DIMENSIONS

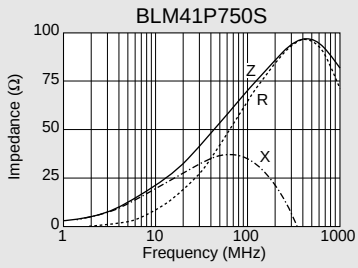


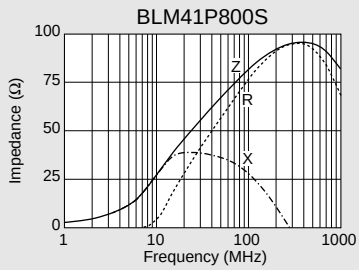
■IMPEDANCE-FREQUENCY CHARACTERISTICS (TYPICAL)

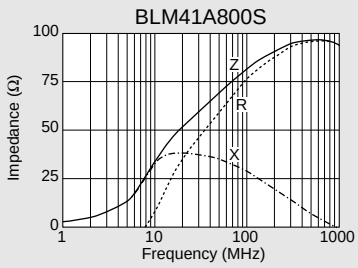


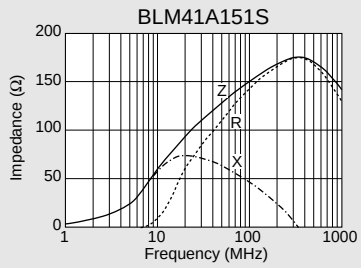
■IMPEDANCE-FREQUENCY CHARACTERISTICS (DETAILS)











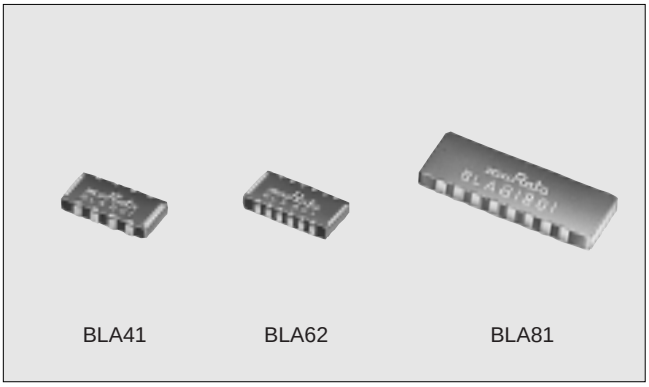
CHIP EMIFIL®

muRata

Chip Ferrite Bead Inductor Array BLA41/62/81 Series

Chip Type Bead Array
(4, 6 or 8 circuits are included in one package.)

The BLA series of chip ferrite bead inductors is designed for surface mount applications. 4, 6, or 8 circuits are condensed into one package to enable significant savings in mounting space.
The inductors feature Murata's original EMI suppression technology as well as an improved design base over the single circuit type BLM series. The series is well suited for EMI suppression in digital I/O lines of varied electronic equipment such as Notebook PCs.



■FEATURES

1. 4, 6, or 8 circuits are available in single packages with either 1.27mm (BLA81/41) or 0.8mm (BLA62) pitch, making the series excellent for the high density EMI suppression requirement.
2. The series can be applied to various situations by two type impedance characteristics, standard type (70Ω at 100MHz) and high-impedance type (600Ω at 100MHz).
3. The series has a unique internal structure that minimizes crosstalk.
4. The nickel barrier structure of the external electrodes provides excellent solder heat resistance.

■APPLICATIONS

- Computers and peripherals, digital TVs, digital VCRs, etc.

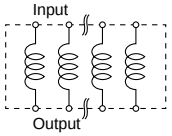
■PART NUMBERING

(Please specify the part number when ordering.)

(Ex.) **BLA** | **62** | **B01** | **T1**
❶ ❷ ❸ ❹

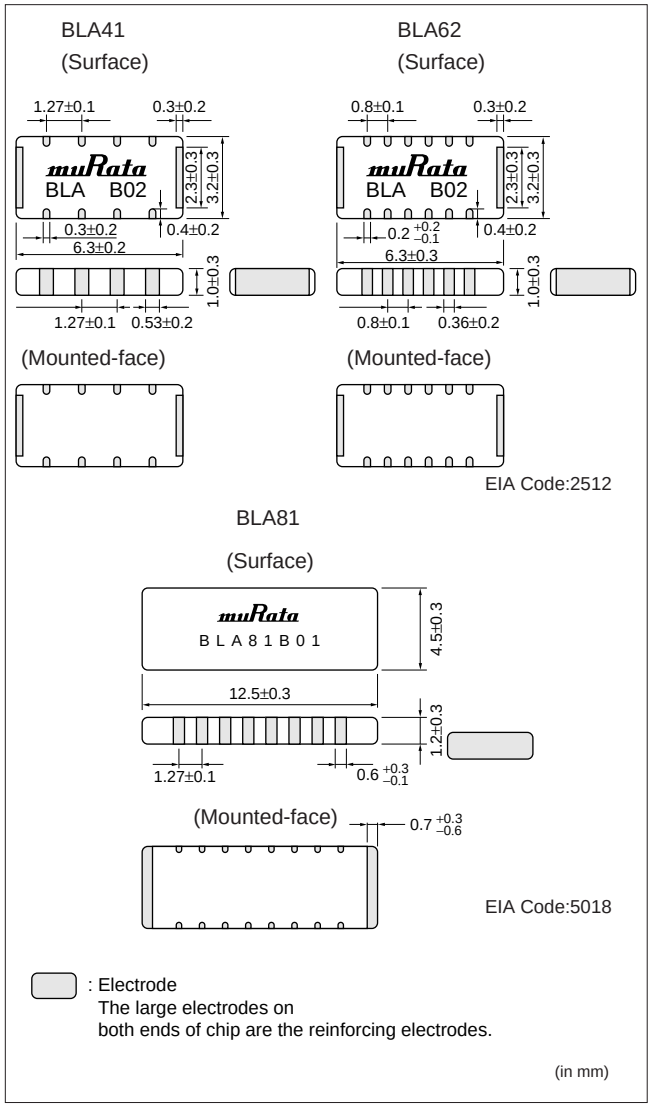
❶Type
❷Number of Circuits and Terminal Pitch
81····8 circuit 1.27mm pitch
62····6 circuit 0.80mm pitch
41····4 circuit 1.27mm pitch
❸Characteristics
❹Packaging Code T1 : Taped
B1 : Bulk package

■EQUIVALENT CIRCUIT DIAGRAM



The BLA series has no polarity.

■DIMENSIONS



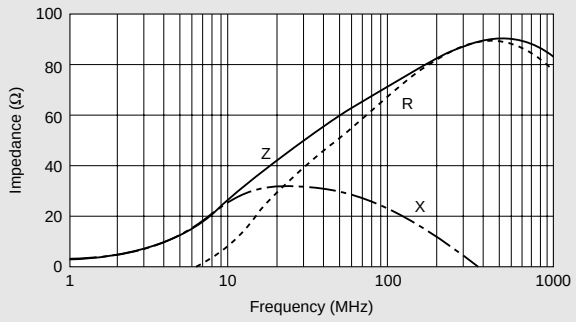
■SPECIFICATIONS

Part Number	Impedance (Ω Typ.) at 100MHz	Rated Current (mA)	Operating Temp. Range (˚C)	Number of Circuits
BLA41B01	70	200	−55 to +125	4
BLA41B02	600	150✻		4
BLA62B01	70	200		6
BLA62B02	600	100✻		6
BLA81B01	70	300		8

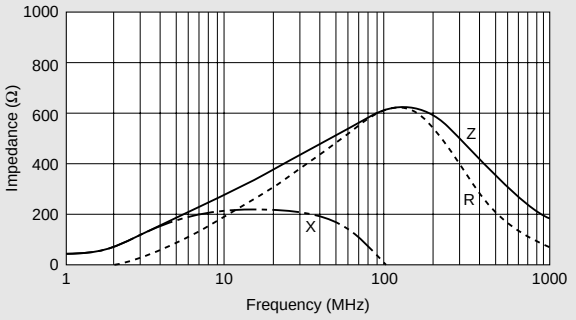
✻BLA41B02/BLA62B02 : Please derate the maximum current, as shown below, for temperatures above +85˚C.

■IMPEDANCE-FREQUENCY CHARACTERISTICS
(TYPICAL)

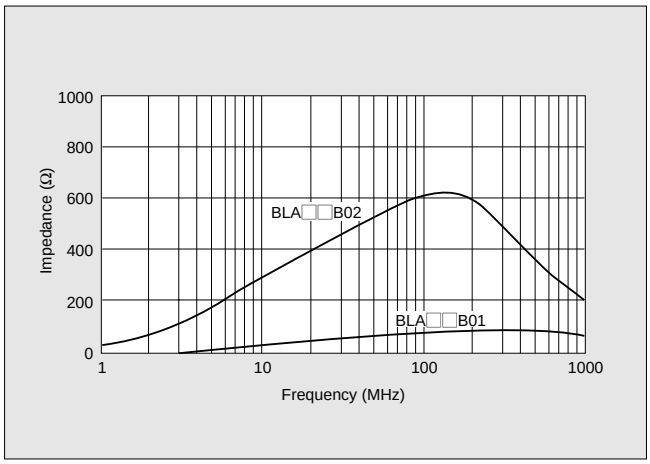
BLA41/62/81B01



BLA41/62B02

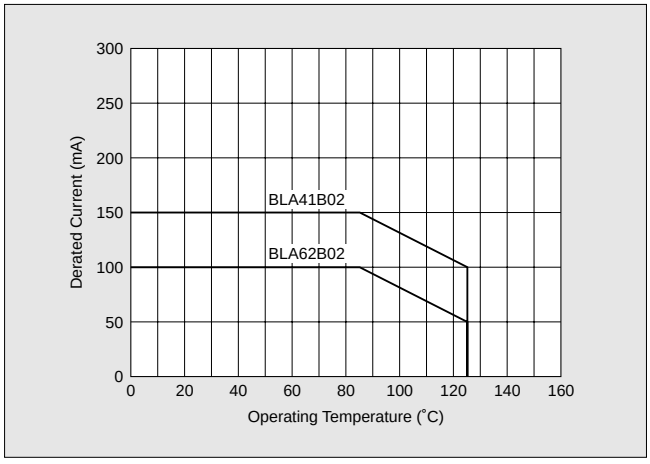


● Comparison between BLA□□B01 with BLA□□B02

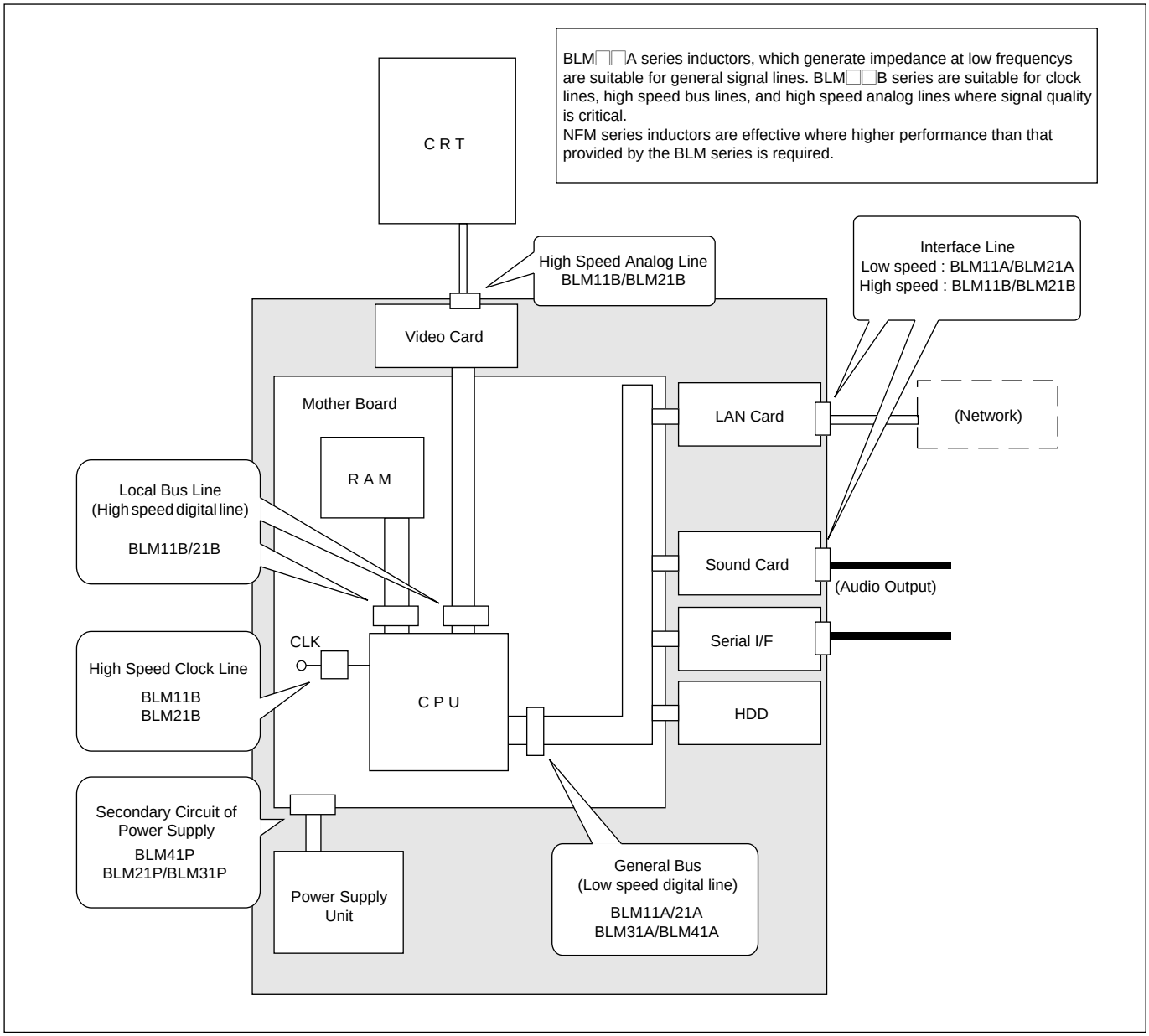


■DERATING

When the BLA41B02/BLM62B02 are used in operating temperature over 85˚C, derating of current is necessary. Please apply the derating curve shown below according to the operating temperature.



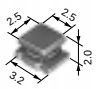
■EXAMPLE OF EMI SUPPRESSION IN PERSONAL COMPUTERS USING THE BLM SERIES



■CHIP INDUCTOR FOR CHOKE USE

There are chip inductors for choke use which are effective to suppress power line noise. Please find most suitable product in wide chip inductor for choke variation.

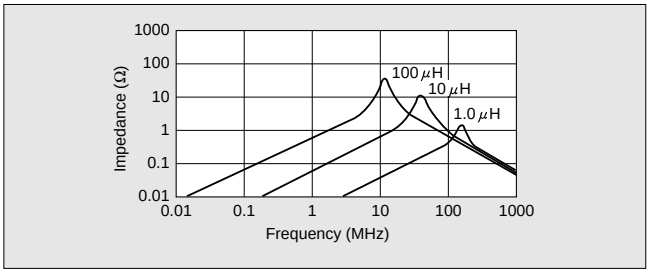
LQH3C



(in mm)

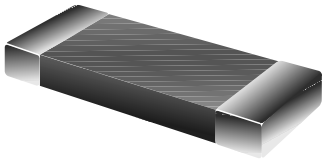
Part Number	Inductance (μH)	DC Resistance ($\Omega\pm30\%$)	Self-resonant Frequency (MHz min.)	Allowable Current (mA)
LQH3C○○○□34	1.0—560	0.09—22.0	5.0—96	60—800
LQH3C○○○□24	0.15—10	0.028—0.30	26—400	450—1450

● **Impedance-Frequency Characteristics** (Typical)



Multilayer Ceramic Chip Capacitors

Type: ECU



■ Features

- Small in size and wide capacitance range
- Superior humidity characteristics and long life thanks to the monolithic construction
- Excellent solderability and resistance to soldering heat thanks to terminals with three (3) layers of silver, nickel, and solder
- Low self-inductance and excellent frequency characteristics

■ Recommended Applications

Class 1 (T.C. Type)

- Temperature compensations, tuned circuits and filter circuits, where low loss and high stability of capacitance and high insulation resistance is required

Class 2 (Hi-K Type)

- Coupling and bypass, where low loss and high stability of capacitance is not so important.

■ Explanation of Part Numbers

1	2	3	4	5	6	7	8	9	10	11	12
E	C	U	X	1	H	1	0	1	J	C	G
Product Code			Packaging Styles	Rated Voltage		Nominal Capacitance			Capacitance Tolerance	Temp. Characteristics	Temp. Characteristics

Product Code	
ECU	Multilayer Ceramic Chip Capacitors

Packaging Styles	
X	Bulk
E	Paper taping (Pitch: 2mm)
V	Paper taping (Pitch: 4mm)
Y	Embossed taping (Pitch: 4mm)
W	Large Size Reel Taping (Pitch: 2mm)
Z	Large Size Reel Taping (Pitch: 4mm)
C	Bulk case

Rated Voltage	
1H	50 VDC
1E	25 VDC
1C	16 VDC

Nominal Capacitance	
0R5	0.5 pF
010	1 pF
100	10 pF
101	100 pF
104	100,000 pF (0.1 µF)

Capacitance Tolerance	
C	±0.25 pF
D	± 0.5 pF
F	± 1 pF
J	± 5%
K	±10%
M	±20%
Z	+80/–20%

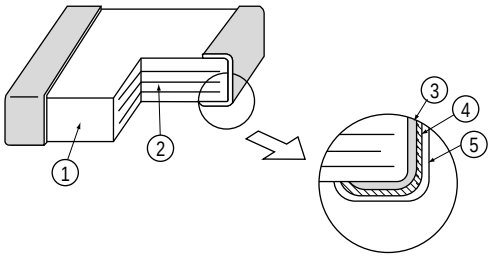
Temp. Characteristics	
C	NPO
P	N150
R	N220
S	N330
T	N470
U	N750
Nil*	SL/GP
B	B/X7R
F	F/Y5V

* When omitted, the remaining P/N factors will be moved up respectively.

Temp. Characteristics		
Q	10 type	0402
V	11 type	0603
N/G	12 type	0805
X**	12 type	
M/H	13 type	1206
W**	13 type	

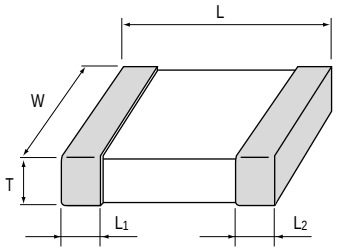
** Extended capacitance range products

■ Construction



No.	Name	Material
①	Ceramic diectric	Ceramic
②	Inner electrode	Palladium
③	Substrate electrode	Silver
③	Intermediate electrode	Nickel
⑤	External electrode	Solder (Pb-Sn)

■ Dimensions in mm (not to scale)



Size Code (EIA)	L	W	T	L_1, L_2
"10" Type (0402)	1.00±0.05	0.50±0.05	0.50±0.05	0.20±0.01
"11" Type (0603)	1.60±0.10	0.80±0.10	0.80±0.10	0.30±0.20
"12" Type (0805)	2.00±0.10	1.25±0.10	1.35 max.*	0.50±0.25
"13" Type (1206)	3.20±0.15	1.60±0.15	1.25 max.*	0.60±0.30

* Specified by nominal capacitance

■ Capacitance Range in pF

Class	Size Code	Dim. "T" (mm)	Capacitance Range (pF) {50 VDC]						
			NPO	SL/GP	N150	N220	N330	N470	N750
			CΔ		PΔ	RΔ	SΔ	TΔ	UΔ
			(CΔJ)*	(SLJ)*	(PΔJ)*	(RΔJ)*	(SΔJ)*	(TΔJ)*	(UΔJ)*
1 (T.C. Type)	"10"	0.50±0.05	0.5–220	0.5–220	0.5–39	0.5–39	0.5–39	0.5–39	0.5–120
	"11" (0603)	0.80±0.10	0.5–1,000	0.5–1,200	0.5–150	0.5–180	0.5–180	0.5–220	0.5–1,200
	"12" (0805)	0.06±0.01	0.5–2,200	0.5–2,700	0.5–220	0.5–220	0.5–220	0.5–270	0.5–2,700
		0.85±0.10	2,400; 2,700	—	240–330	240–390	240–470	300–470	—
		1.25±0.10	—	—	360–470	430–560	510, 560	510–680	—
	"13" (1206)	0.6±0.1	0.5–4,700	0.5–5,600	0.5–560	0.5–680	0.5–680	0.5–820	0.5–5,600
		0.85±0.10	5,100–6,800	—	620–1,200	750–1,200	750–1,500	910–1,500	—
		1.15±0.10	7,500–10,000	—	1,300; 1,500	1,300; 1,500	1,600; 1,800	1,600–2,200	—

Class	Size Code	Dim. "T" (mm)	Capacitance Range (pF) {50 VDC]					
			B/(RB)*/X7R		B/(BJ)*/Y5P	F/(FJ)*/Y5V		
			50 VDC	25 VDC	16 VDC	50 VDC	25 VDC	16 VDC
2 (Hi-K Type)	"10" (0402)	0.50±0.05	—	100–4,700	5,600–15,000	—	1,000–10,000	15,000–100,000
	"11" (0603)	0.80±0.10	220–15,000	18,000–33,000	10,000–100,000	1,000–47,000	68,000; 100,000	100,000–470,000
	"12" (0805)	0.6±0.1	220–22,000	18,000–33,000	—	1,000–68,000	68,000–150,000	100,000–220,000
		0.85±0.10	27,000–39,000	39,000–100,000	47,000–220,000	100,000	220,000	330,000–1M
	"13" (1206)	0.6±0.1	220–56,000	33,000–82,000	—	1,000–220,000	100,000–470,000	—
		0.85±0.10	68,000–100,000	100,000–220,000	100,000–680,000	—	—	680,000–2.2M
		1.5±0.10	—	—	820,000–1M	—	—	—

* Temperature characteristics codes conform to JIS C6429

■ Nominal Capacitance vs. Capacitance Tolerance

Tolerance Code	Capacitance Tolerance		Nominal Capacitance Available		Temp. Char.	Class
C	≤10 pF	±0.25 pF	0.5, 1, 1.5, 2, 3, 4, 5		CD to UD (NPO) (N750) and SL/GP	1 (T.C. Type)
D		±0.05 pF	1, 1.5, 2, 3, 4, 5, 6, 7, 8, 9, 10			
F		±1.0 pF	10			
J	>10 pF	±5%	E24	Within capacitance range, E-series number x 10^n		
K		±10%	E12			
K	±10%		E12		B (X7R)	2 (Hi-K Type)
M	±20%		E6			
Z	+80, –20%		E6		F (Y5V)	

■ E-Series Numbers

E6	1				1.5				2.2				3.3				4.7				6.8			
E12	1		1.2		1.5		1.8		2.2		2.7		3.3		3.9		4.7		5.6		6.8		8.2	
E24	1	1.1	1.2	1.3	1.5	1.6	1.8	2	2.2	2.4	2.7	3	3.3	3.6	3.9	4.3	4.7	5.1	5.6	6.2	6.8	7.5	8.2	9.1

■ Temperature Coefficient of Class 1 Capacitors/T.C. Tolerance

		Temperature Coefficient Code.						
T.C.	**Cap.**	**CΔ (NPO)**	**PΔ (N150)**	**RΔ (N220)**	**SΔ (N330)**	**TΔ (N470)**	**UΔ (N750)**	**SL/GP**
T.C. Tol.	≤2 pF	CK (±250)	PK (±250)	RK (±250)	SK (±250)	TK (±250)	UK (±250)	+350 to –1000
	3 pF	CJ (±120)	PJ (±120)	RJ (±120)	SJ (±120)	TJ (±120)	UJ (±120)	+350 to –1000
	≥4 pF	CH (±60)	PH (±60)	RH (±60)	SH (±60)	TH (±60)	UJ (±120)	+350 to –1000

■ Temperature Coefficient of Class 2 Capacitors

	Capacitance Change			
Temp. Char.	**No DC Voltage Applied**	**1/2 Rate Voltage Applied**	**Measurement Temp. Range**	**Reference Temperature**
B (RB)	± 10% max.	+10, –30% max.	–25 to 85°C	20°C
F (FJ)	+30, –80% max.	+30, –95% max.	–25 to 85°C	20°C

■ Base Metal Inner Electrode Type* (Nickel)

Size Code	Capacitance Range (pF) F (FJ)/Y5V)
"11" (0603)	0.1 µF/50 V to 0.33 µF/16V
"12" (0805)	0.01 µF/50 V to 2.2 µF/16V
"13" (1206)	0.22 µF/50V to 4.7 µF/16V

* For details on the new series, please contact us.

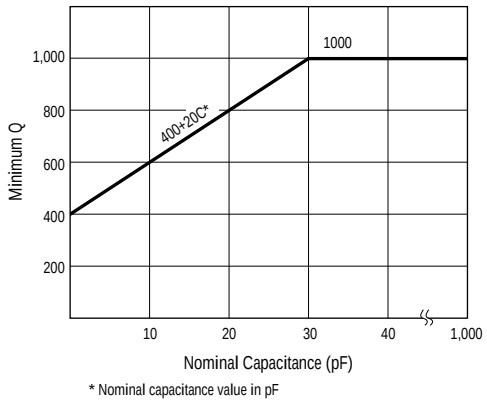
■ Specifications

Characteristics	Specifications				Test Methods
	Class 1 (T.C. Type)	Class 2 (Hi-K Type)			
	CD to UD and SL/GP	B/X7R	B/Y5P	F/Y5V	
Operating temperature range	–55 to 125°C*		–25 to 80°C		—
Rated voltage	50 VDC	50 VDC, 25 VDC	16 VDC	50 VDC 25 VDC 16 VDC	—
Dielectric withstanding voltage	No breakdown				Class 1: Rated voltage x 3, 1 to 5 s Class 2: Rated voltage x 2.5, 1 to 5 s Limit surge current: 50 mA max.
Insulation resistance (R)	IR≥10,000MΩ or 500/C** MΩ whichever is less (C: Rated capacitance in μF)				Rated voltage at 1 minute electrification
Capacitance	Within the specified tolerance				
Q Factor or Dissipation Factor (tan δ)	Capacitance < 30 pF Q ≥ 400+ 20C*** 30 pF ≤ Cap. ≤ 1000 pF Q ≥ 1000 Capacitance > 1000 pF D.F. (tan δ) ≤0.002	D.F. (tan δ) ≤0.025		D.F. (tan δ) ≤0.05	

Class		Frequency	Voltage	Temp.
1	≤1000 pF	1 MH ±10%	0.5 to 5 Vrms	20°C
	>1000 pF	1 kHz ±10%		
2		1 kHz ±10%	1±0.2 Vrms	

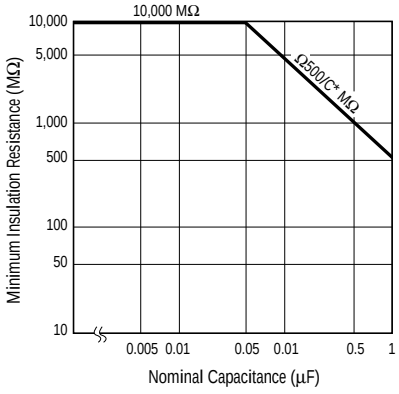
* Operating temperature range: –25 to 80 °C for capacitance of 5100 to 1000 pF, NP0, Type 13.
** Nominal capacitance value in μF
*** Nominal capacitance value in pF

Minimum Q at 1 MHz



* Nominal capacitance value in pF

Minimum Insulation Resistance



* Nominal capacitance value in pF

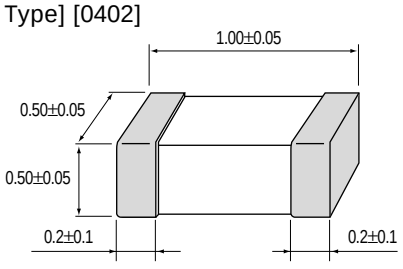
■ Capacitance Range (in pF)
[Size Code “10” Type/“0402”]

Cap. (pF)	CΔ (NPO) 50V	SL/GP 50V	PΔ (N150) 50V	RΔ (N220) 50V	SΔ (N330) 50V	TΔ (N470) 50V	UΔ (N750) 50V
0.5							
1							
1.5							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11			Q	Q	Q	Q	
12							
13							
15							
16							
18							
20							
22							Q
24							
27	Q	Q					
30							
33							
36							
39							
43							
47							
51							
56							
62							
68							
75							
82							
91							
100							
110							
120							
130							
150							
160							
180							
200							
220							

Note: The Q in the table above indicates the suffix code in “Explanation of Part Numbers” table.

Cap. (pF)	B/X7R 25V	B/Y5P 16V	F/Y5V 25V	F/Y5V 16V
100				
120				
150				
180				
220				
270				
330				
390				
470				
560				
680	Q			
820				
1,000			Q	
1,200				
1,500			Q	
1,800				
2,200			Q	
2,700				
3,300			Q	
3,900				
4,700			Q	
5,600				
6,800			Q	
8,200		Q		
10,000			Q	
12,000				
15,000				Q
18,000				
22,000				Q
27,000				
33,000				Q
39,000				
47,000				Q
56,000				
68,000				Q
82,000				
100,000				Q

Dimensions in mm (not to scale)
[10 Type] [0402]



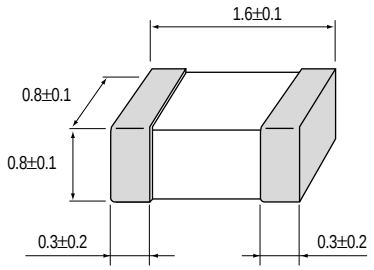
■ Capacitance Range (in pF)
[Size code “11” Type/“0603” (EIA)]

Cap. (pF)	CΔ (NPO) 50V	SL/GP 50V	PΔ (N150) 50V	RΔ (N220) 50V	SΔ (N330) 50V	TΔ (N470) 50V	UΔ (N750) 50V
0.5	V	V	V	V	V	V	V
1	V	V	V	V	V	V	V
1.5	V	V	V	V	V	V	V
2	V	V	V	V	V	V	V
3	V	V	V	V	V	V	V
4	V	V	V	V	V	V	V
5	V	V	V	V	V	V	V
6	V	V	V	V	V	V	V
7	V	V	V	V	V	V	V
8	V	V	V	V	V	V	V
9	V	V	V	V	V	V	V
10	V	V	V	V	V	V	V
11	V	V	V	V	V	V	V
12	V	V	V	V	V	V	V
13	V	V	V	V	V	V	V
15	V	V	V	V	V	V	V
16	V	V	V	V	V	V	V
18	V	V	V	V	V	V	V
20	V	V	V	V	V	V	V
22	V	V	V	V	V	V	V
24	V	V	V	V	V	V	V
27	V	V	V	V	V	V	V
30	V	V	V	V	V	V	V
33	V	V	V	V	V	V	V
36	V	V	V	V	V	V	V
39	V	V	V	V	V	V	V
43	V	V	V	V	V	V	V
47	V	V	V	V	V	V	V
51	V	V	V	V	V	V	V
56	V	V	V	V	V	V	V
62	V	V	V	V	V	V	V
68	V	V	V	V	V	V	V
75	V	V	V	V	V	V	V
82	V	V	V	V	V	V	V
91	V	V	V	V	V	V	V
100	V	V	V	V	V	V	V
110	V	V	V	V	V	V	V
120	V	V	V	V	V	V	V
130	V	V	V	V	V	V	V
150	V	V	V	V	V	V	V
160	V	V	V	V	V	V	V
180	V	V	V	V	V	V	V
200	V	V	V	V	V	V	V
220	V	V	V	V	V	V	V
240	V	V	V	V	V	V	V
270	V	V	V	V	V	V	V
300	V	V	V	V	V	V	V
330	V	V	V	V	V	V	V
360	V	V	V	V	V	V	V
390	V	V	V	V	V	V	V
430	V	V	V	V	V	V	V
470	V	V	V	V	V	V	V
510	V	V	V	V	V	V	V
560	V	V	V	V	V	V	V
620	V	V	V	V	V	V	V
680	V	V	V	V	V	V	V
750	V	V	V	V	V	V	V
820	V	V	V	V	V	V	V
910	V	V	V	V	V	V	V
1,000	V	V	V	V	V	V	V
1,100	V	V	V	V	V	V	V
1,200	V	V	V	V	V	V	V

Cap. (pF)	B/X7R 25V	B/X7R 25V	B/Y5P 16V	F/Y5V 50V	F/Y5V 25V	F/Y5V 16V
220	V					
270	V					
330	V					
390	V					
470	V					
560	V					
680	V					
820	V					
1,000	V			V		
1,200	V			V		
1,500	V			V		
1,800	V			V		
2,200	V			V		
2,700	V			V		
3,300	V			V		
3,900	V			V		
4,700	V			V		
5,700	V			V		
6,800	V			V		
8,200	V		V	V		
10,000	V		V	V		
12,000	V		V	V		
15,000	V		V	V		
18,000		V	V	V		
22,00		V	V	V		
27,000		V	V	V		
33,000		V	V	V		
39,000		V	V	V		
47,000		V	V	V		
56,000		V	V		V	
68,000		V	V		V	
82,000		V	V		V	
100,000		V	V		V	V
120,000		V	V		V	V
150,000		V	V		V	V
180,000		V	V		V	V
220,000		V	V		V	V
270,000		V	V		V	V
330,000		V	V		V	V
390,000		V	V		V	V
470,000		V	V		V	V

Note: The V in the table above indicates the suffix code in “Explanation of Part Numbers” table.

Dimensions in mm (not to scale)
[11 Type] [0603 (EIA)]



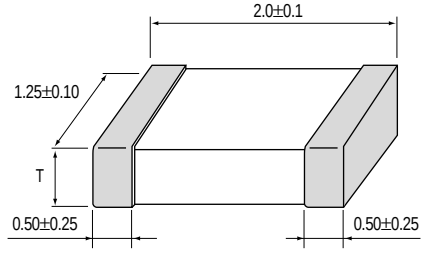
■ Capacitance Range (in pF)
[Size Code “12” Type/“0805” (EIA)]

Cap. pF	CΔ (NPO) 50V	SL/GP 50V	PΔ (N150) 50V	RΔ (N220) 50V	SΔ (N330) 50V	TΔ (N470) 50V	UΔ (N750) 50V
0.5	N	N	N	N	N	N	N
1	N	N	N	N	N	N	N
1.5	N	N	N	N	N	N	N
2	N	N	N	N	N	N	N
3	N	N	N	N	N	N	N
4	N	N	N	N	N	N	N
5	N	N	N	N	N	N	N
6	N	N	N	N	N	N	N
7	N	N	N	N	N	N	N
8	N	N	N	N	N	N	N
9	N	N	N	N	N	N	N
10	N	N	N	N	N	N	N
11	N	N	N	N	N	N	N
12	N	N	N	N	N	N	N
13	N	N	N	N	N	N	N
15	N	N	N	N	N	N	N
16	N	N	N	N	N	N	N
18	N	N	N	N	N	N	N
20	N	N	N	N	N	N	N
22	N	N	N	N	N	N	N
24	N	N	N	N	N	N	N
27	G	G	N	N	N	N	N
30	G	G	N	N	N	N	N
33	G	G	N	N	N	N	N
36	G	G	N	N	N	N	N
39	G	G	N	N	N	N	N
43	G	G	N	N	N	N	N
47	G	G	N	N	N	N	N
51	G	G	N	N	N	N	N
56	G	G	N	N	N	N	N
62	G	G	N	N	N	N	N
68	G	G	N	N	N	N	N
75	G	G	N	N	N	N	N
82	G	G	N	N	N	N	N
91	G	G	N	N	N	N	N
100	G	G	N	N	N	N	N
110	G	G	N	N	N	N	N
120	G	G	N	N	N	N	N
130	G	G	N	N	N	N	N
150	G	G	N	N	N	N	N
160	G	G	N	N	N	N	N
180	G	G	N	N	N	N	N
200	G	G	N	N	N	N	N
220	G	G	N	N	N	N	N
240	G	G	N	N	N	N	N
270	G	G	N	N	N	N	N
300	G	G	N	N	N	N	N
330	G	G	N	N	N	N	N
360	G	G	N	N	N	N	N
390	G	G	N	N	N	N	N
430	X	G	N	N	N	N	X
470	X	G	N	N	N	N	X
510	X	G	N	N	N	N	X
560	X	G	N	N	N	N	X
620	X	G	N	N	N	N	X
680	X	G	N	N	N	N	X
750	X	G	N	N	N	N	X
820	X	G	N	N	N	N	X
910	X	G	N	N	N	N	X
1,000	X	G	N	N	N	N	X
1,100	X	G	N	N	N	N	X
1,200	X	G	N	N	N	N	X
1,300	X	G	N	N	N	N	X
1,500	X	G	N	N	N	N	X
1,600	X	G	N	N	N	N	X
1,800	X	G	N	N	N	N	X
2,000	X	G	N	N	N	N	X
2,200	X	G	N	N	N	N	X
2,400	X	G	N	N	N	N	X
2,700	X	G	N	N	N	N	X

Cap. (pF)	B/X7R 25V	B/X7R 25V	B/Y5P 16V	F/Y5V 50V	F/Y5V 25V	F/Y5V 16V
220	N					
270	N					
330	N					
390	N					
470	N					
560	N					
680	N					
820	N					
1,000	N			N		
1,200	N			N		
1,500	N			N		
1,800	N			N		
2,200	N			N		
2,700	N			N		
3,300	N			N		
3,900	N			N		
4,700	G			N		
5,600	G			N		
6,800	G			N		
8,200	G			N		
10,000	G			G		
12,000	G			G		
15,000	X			G		
18,000	X			G		
22,000	X	G		G		
27,000	X	G		X		
33,000	X	G		X		
39,000	X	G		X		
47,000	X	G		X		
56,000	X	G		X		
68,000	X	G		X	X	
82,000	X	G		C	X	X
100,000	X	G		C	X	X
120,000	X	G		C	X	X
150,000	X	G		C	X	X
180,000	X	G		C	X	X
220,000	X	G		C	X	X
270,000	X	G		C	X	X
330,000	X	G		C	X	X
390,000	X	G		C	X	X
470,000	X	G		C	X	X
560,000	X	G		C	X	X
680,000	X	G		C	X	X
820,000	X	G		C	X	X
1,000,000	X	G		C	X	X

Note: The N, G, X, and C in above table indicate the suffix codes in “Explanation of Part Numbers” chart.

Dimensions in mm (not to scale)
[12 Type] [0805 (EIA)]



Thickness “T” (mm)

0.6±0.1 0.85±0.10 1.15±0.10

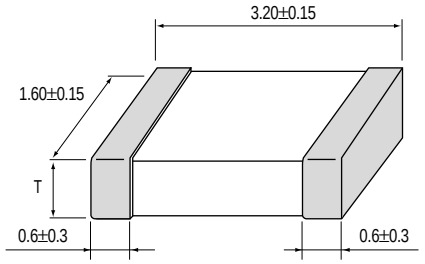
■ Capacitance Range (in pF)
[Size Code “13” Type/“1206” (EIA)]

Cap. pF)	CΔ (NPO) 50V	SL/GP 50V	PΔ (N150) 50V	RΔ (N220) 50V	SΔ (N330) 50V	TΔ (N470) 50V	UΔ (N750) 50V
0.5	M	M	M	M	M	M	M
1	M	M	M	M	M	M	M
1.5	M	M	M	M	M	M	M
2	M	M	M	M	M	M	M
3	M	M	M	M	M	M	M
4	M	M	M	M	M	M	M
5	M	M	M	M	M	M	M
6	M	M	M	M	M	M	M
7	M	M	M	M	M	M	M
8	M	M	M	M	M	M	M
9	M	M	M	M	M	M	M
10	M	M	M	M	M	M	M
11	M	M	M	M	M	M	M
12	M	M	M	M	M	M	M
13	M	M	M	M	M	M	M
15	M	M	M	M	M	M	M
16	M	M	M	M	M	M	M
18	M	M	M	M	M	M	M
20	M	M	M	M	M	M	M
22	M	M	M	M	M	M	M
24	M	M	M	M	M	M	M
27	M	M	M	M	M	M	M
30	M	M	M	M	M	M	M
33	M	M	M	M	M	M	M
36	M	M	M	M	M	M	M
39	M	M	M	M	M	M	M
43	M	M	M	M	M	M	M
47	M	M	M	M	M	M	M
61	M	M	M	M	M	M	M
56	M	M	M	M	M	M	M
62	M	M	M	M	M	M	M
68	M	M	M	M	M	M	M
75	M	M	M	M	M	M	M
82	M	M	M	M	M	M	M
91	M	M	M	M	M	M	M
100	M	M	M	M	M	M	M
110	M	M	M	M	M	M	M
120	M	M	M	M	M	M	M
130	M	M	M	M	M	M	M
150	M	M	M	M	M	M	M
160	M	M	M	M	M	M	M
180	M	M	M	M	M	M	M
200	H	M	M	M	M	M	M
220	H	M	M	M	M	M	M
240	H	M	M	M	M	M	M
270	H	M	M	M	M	M	M
300	H	M	M	M	M	M	M
330	H	M	M	M	M	M	M
360	H	M	M	M	M	M	M
390	H	M	M	M	M	M	M
430	H	M	M	M	M	M	M
470	H	M	M	M	M	M	M
510	H	M	M	M	M	M	M
560	H	M	M	M	M	M	M
620	H	M	M	M	M	M	M
680	H	M	M	M	M	M	M
750	H	M	M	M	M	M	M
820	H	M	M	M	M	M	M
910	H	M	M	M	M	M	M
1,000	H	M	M	M	M	M	M
1,100	H	M	M	M	M	M	M
1,200	H	M	M	M	M	M	M
1,300	H	M	M	M	M	M	M
1,500	H	M	M	M	M	M	M
1,600	H	M	M	M	M	M	M
1,800	H	M	M	M	M	M	M
2,000	H	M	M	M	M	M	M
2,200	H	M	M	M	M	M	M
2,400	H	M	M	M	M	M	M
2,700	H	M	M	M	M	M	M
3,000	H	M	M	M	M	M	M
3,300	H	M	M	M	M	M	M
3,600	H	M	M	M	M	M	M
3,900	H	M	M	M	M	M	M
4,300	H	M	M	M	M	M	M
4,700	H	M	M	M	M	M	M
5,100	X	M	M	M	M	M	M
5,600	X	M	M	M	M	M	M
6,200	X	M	M	M	M	M	M
6,800	X	M	M	M	M	M	M
7,500	X	M	M	M	M	M	M
8,200	W	M	M	M	M	M	M
9,100	W	M	M	M	M	M	M
10,000	W	M	M	M	M	M	M

Cap. (pF)	B/X7R 25V	B/X7R 25V	B/Y5P 16V	F/Y5V 50V	F/Y5V 25V	F/Y5V 16V
220	M					
270	M					
330	M					
390	M					
470	M					
560	M					
680	M					
820	M					
1,000	M			N		
1,200	M			M		
1,500	M			M		
1,800	M			M		
2,200	M			M		
2,700	M			M		
3,300	M			M		
3,900	M			M		
4,700	M			M		
5,600	M			M		
6,800	M			M		
8,200	M			M		
10,000	M			M		
12,000	M			M		
15,000	M			M		
18,000	M			M		
22,000	M			M		
27,000	W	W		M		
33,000	W	W		M		
39,000	W	W		M		
47,000	W	W		W		
56,000	W	W		W		
68,000	W	W		W		
82,000	W	W		W		
100,000	W	W		W	W	
120,000	W	W		W	W	
150,000	W	W		W	W	
180,000	W	W		W	W	
220,000	W	W		W	W	
270,000	W	W	X	W	W	
330,000	W	W	X	W	W	
390,000	W	W	X	W	W	
470,000	W	W	X	W	W	
560,000	W	W	X	W	W	
680,000	W	W	X	W	W	W
820,000	W	W	X	W	W	W
1,000,000	W	W	X	W	W	W
1,200,000	W	W	X	W	W	W
1,500,000	W	W	X	W	W	W
1,800,000	W	W	X	W	W	W
2,200,000	W	W	X	W	W	W

Note: The M, H, and W in above table indicate the suffix does in “Explanation of Part Numbers” chart.

Dimensions in mm (not to scale)
[13 Type] [1206 (EIA)]



Thickness “T” (mm)

0.6±0.1 0.85±0.10 1.15±0.10

■ Standard Products for "10" Type (EIA "0402" Type), Taped Version
[Rated voltage 50 VDC]
Dim. T (mm) = 0.5

Cap. (pF)	Cap. Tol.	Part Number						
		CΔ (NPO)	SL/GP	PΔ (N150)	RΔ (N220)	SΔ (N330)	TΔ (N470)	UΔ (N750)
0.5	±0.25 pF(C)	ECUE1H0R5CCQ	ECUE1H0R5CQ	ECUE1HR5CPQ	ECUE1H0R5CRQ	ECUE1H0R5CSQ	ECUE1H0R5CTQ	ECUE1H0R5CUQ
1	0.25 pF (C) or ±0.5 pF (D)	ECUE1H010✻CQ	ECUE1H010✻Q	ECUE1H010✻PQ	ECUE1H010✻RQ	ECUE1H010✻SQ	ECUE1H010✻TQ	ECUE1H010✻UQ
1.5		ECUE1H1R5✻CQ	ECUE1H1R5✻Q	ECUE1H1R5✻PQ	ECUE1H1R5✻RQ	ECUE1H1R5✻SQ	ECUE1H1R5✻TQ	ECUE1H1R5✻UQ
2		ECUE1H020✻CQ	ECUE1H020✻Q	ECUE1H020✻PQ	ECUE1H020✻RQ	ECUE1H020✻SQ	ECUE1H020✻TQ	ECUE1H020✻UQ
3		ECUE1H030✻CQ	ECUE1H030✻Q	ECUE1H030✻PQ	ECUE1H030✻RQ	ECUE1H030✻SQ	ECUE1H030✻TQ	ECUE1H030✻UQ
4		ECUE1H040✻CQ	ECUE1H040✻Q	ECUE1H040✻PQ	ECUE1H040✻RQ	ECUE1H040✻SQ	ECUE1H040✻TQ	ECUE1H040✻UQ
5	±0.5 pF (D)	ECUE1H050✻CQ	ECUE1H050✻Q	3CUE1H050✻PQ	ECUE1H050✻RQ	ECUE1H050✻SQ	ECUE1H050✻TQ	ECUE1H050✻UQ
6		ECUE1H060DCQ	ECUE1H060DQ	ECUE1H060DPQ	ECUE1H060DRQ	ECUE1H060DSQ	ECUE1H060DTQ	ECUE1H060DUQ
7		ECUE1H070DCQ	ECUE1H070DQ	ECUE1H070DPQ	ECUE1H070DRQ	ECUE1H070DSQ	ECUE1H070DTQ	ECUE1H070DUQ
8		ECUE1H080DCQ	ECUE1H080DQ	ECUE1H080DPQ	ECUE1H080DRQ	ECUEQH080DSQ	ECUE1H080DTQ	ECUE1H080DUQ
9		ECUE1H090DCQ	ECUE1H090DQ	ECUE1H090DPQ	ECUE1H090DRQ	ECUE1H090DSQ	ECUE1H090DTQ	ECUE1H090DUQ
10	±0.5 pF (D) or ±1 pf (F)	ECUE1H100✻CQ	ECUE1H100✻Q	ECUE1H100✻PQ	ECUE1H100✻RQ	ECUE1H100✻SQ	ECUE1H100✻TQ	ECUE1H100✻UQ
11	±5%*** (J) or ±10% (K)	ECUE1H110JCQ	ECUE1H110JQ	ECUE1H110JPQ	ECUE1H110JRQ	ECUE1H110✻SQ	ECUE1H110JTQ	ECUE1H110JUQ
12		ECUE1H120✻CQ	ECUE1H120✻Q	ECUE1H120✻PQ	ECUE1H120✻RQ	ECUE1H110JSQ	ECUE1H120✻TQ	ECUE1H120✻UQ
13		ECUE1H130JCQ	ECUE1H130JQ	ECUE1H130JPQ	ECUE1H130JRQ	ECUE1H120✻SQ	ECUE1H130JQT	ECUE1H130JUQ
15		ECUE1H150✻CQ	ECUE1H150✻Q	ECUE1H150✻PQ	ECUE1H150✻RQ	ECUE1H130JSQ	ECUE1H150✻TQ	ECUE1H150✻UQ
16		ECUE1H160JCQ	ECUE1H160✻Q	ECUE1H160JPQ	ECUE1H160JRQ	ECUE1H150✻SQ	ECUE1H160JTQ	ECUE1H160JUQ
18		ECUE1H180✻CQ	ECUE1H180✻Q	ECUE1H180✻PQ	ECUE1H180✻RQ	ECUE1H160JSQ	ECUE1H180✻TQ	ECUE1H180✻UQ
20		ECUE1H200JCQ	ECUE1H200JQ	ECUE1H200JPQ	ECUE1H200JRQ	ECUE1H180✻SQ	ECUE1H200JTQ	ECUE1H200JUQ
22		ECUE1H220✻CQ	ECUE1H220✻Q	ECUE1H220✻PQ	ECUE1H220✻RQ	ECUE1H200JSQ	ECUE1H220✻TQ	ECUE1H220✻UQ
24		ECUE1H240JCQ	ECUE1H240JQ	ECUE1H240JPQ	ECUE1H240JRQ	ECUE1H220✻SQ	ECUE1H240JTQ	ECUE1H240JUQ
27		ECUE1H270✻CQ	ECUE1H270✻Q	ECUE1H240✻PQ	ECUE1H270✻RQ	ECUE1H240JSQ	ECUE1H270✻TQ	ECUE1H270✻UQ
30		ECUE1H300JCQ	ECUE1H300JQ	ECUE1H300JPQ	ECUE1H300JRQ	ECUE1H270✻SQ	ECUE1H300JTQ	ECUE1H300JUQ
33		ECUE1H330✻CQ	ECUE1H330✻Q	ECUE1H330✻PQ	ECUE1H330✻RQ	ECUE1H300JSQ	ECUE1H330✻TQ	ECUE1H3390✻UQ
36		ECUE1H360JCQ	ECUE1H360JQ	ECUE1H360JPQ	ECUE1H360JRQ	ECUE1H330✻SQ	ECUE1H360JTQ	ECUE1H360JUQ
39		ECUE1H390✻CQ	ECUE1H390✻Q	ECUE1H390✻PQ	ECUE1H390✻RQ	ECUE1H360JSQ	ECUE1H390✻TQ	ECUE1H390✻UQ
43		ECUE1H430JCQ	ECUE1H430JQ			ECUE1H390✻SQ		ECUE1H430JUQ
47		ECUE1H470✻CQ	ECUE1H470✻Q					ECUE1H470✻UQ
51		ECUE1H510JCQ	ECUE1H510JQ					ECUE1H510JUQ
56		ECUE1H560✻CQ	ECUE1H560✻Q					ECUE1H560✻UQ
62		ECUE1H620JCQ	ECUE1H620JQ					ECUE1H620JUQ
68		ECUE1H680✻CQ	ECUE1H680✻Q					ECUE1H680✻UQ
75		ECUE1H750HCQ	ECUE1H750JQ					ECUE1H750JUQ
82		ECUE1H820✻CQ	ECUE1H820✻Q					ECUE1H820✻UQ
91		ECUE1H910JCQ	ECUE1H910JQ					ECUE1H910JUQ
100		ECUE1H101✻CQ	ECUE1H101✻Q					ECUE1H101✻UQ
110		ECUE1H111JCQ	ECUE1H111JQ					ECUE1H111JUQ
120		ECUE1H121✻CQ	ECUE1H121✻Q					ECUE1H121✻UQ
130		ECUE1H131JCQ	ECUE1H131JQ					
150		ECUE1H151✻CQ	ECUE1H141✻Q					
160		ECUE1H161JCQ	ECUE1H161JQ					
180		ECUE1H181✻CQ	ECUE1H181✻Q					
200		ECUE1H201JCQ	ECUE1H201JQ					
220		ECUE1H221✻CQ	ECUE1H221✻Q					

Cap. Tol. Code**

Packing style code*

* Packaging style code: "E" for taped version (taping pitch: 2mm) and "X" for bulk type

** ✻ : Capacitance tolerance codes

*** Capacitance values of "E24" series and capacitance tolerance of ±5% are available on special order.

■ Standard Products for "10" Type (EIA "0402" Type), Taped Version
Dim. T (mm) = 0.5

Cap. (pF)	Capacitance Tolerance	Part Number B/X7R 25 VDC	Part Number B/Y5P 16 VDC	Capacitance Tolerance	Part Number F/Y5V 25 VDC	Part Number F/Y5V 16 VDC
100	±10% (K) or ±20% (M)	ECUE1E101✻BQ		+80/–20% (Z)		
120		ECUE1E121KBQ				
150		ECUE1E151✻BQ				
180		ECUE1E181KBQ				
220		ECUE1E221✻BQ				
270		ECUE1E271KBQ				
330		ECUE1E331✻BQ				
390		ECUE1E391KBQ				
470		ECUE1E471✻BQ				
560		ECUE1E561KBQ				
680		ECUE1E681✻BQ				
820		ECUE1E821KBQ				
1,000		ECUE1E102✻BQ			ECUE1E102ZFQ	
1,200		ECUE1E122KBQ				
1,500		ECUE1E152✻BQ			ECUE1E152ZFQ	
1,800		ECUE1E182KBQ				
2,200		ECUE1E222✻BQ			ECUE1E222ZFQ	
2,700		ECUE1E272KBQ				
3,300		ECUE1E332✻BQ			ECUE1E332ZFQ	
3,900		ECUE1E392KBQ				
4,700		ECUE1E472✻BQ	ECUE1C562KBQ		ECUE1E472ZFQ	
5,600			ECUE1C682✻BQ			
6,800			ECUE1C822KBQ		ECUE1E682ZFQ	
8,200			ECUE1C103✻BQ			
10,000			ECUE1C123KBQ		ECUE1E103ZFQ	
12,000			ECUE1C152✻BQ			
15,000						ECUE1C153ZFQ
18,000						
22,000						ECUE1C223ZFQ
27,000						
33,000						ECUE1C333ZFQ
39,000						
47,000						ECUE1C473ZFQ
56,000						
68,000						ECUE1C683ZFQ
82,000						
100,000						ECUE1C104ZFQ

* ✻ : Capacitance tolerance codes
** Packaging styles code: "E" for taped version (taping pitch: 2mm) and "X" for bulk type)

■ Standard Products for "11" Type (EIA "0603" Type), Taped Version
[Rated voltage 50 VDC]
Dim. T (mm) = 0.8

Cap. (pF)	Cap. Tol.	Part Number						
		CΔ (NPO)	SL/GP	PΔ (N150)	RΔ (N220)	SΔ (N330)	TΔ (N470)	UΔ (N750)
0.5	±0.25 pF(C)	ECUV1H0R5CCV	ECUV1H0R5CV	ECUV1H0R5CPV	ECUV1H0R5CRV	ECUV1H0R5CSV	ECUV1H0R5CSV	ECUV1H0R5CUV
1	0.25 pF (C) or ±0.5 pF (D)	ECUV1H010✻CV	ECUV1H010✻V	ECUV1H010✻PV	ECUV1H010✻RV	ECUV1H010✻SV	ECUV1H010✻TV	ECUV1H010✻UV
1.5		ECUV1H1R5✻CV	ECUV1H1R5✻V	ECUV1H1R5✻PV	ECUV1H1R5✻RV	ECUV1H1R5✻SV	ECUV1H1R5✻TV	ECUV1H1R5✻UV
2		ECUV1H020✻CV	ECUV1H020✻V	ECUV1H020✻PV	ECUV1H020✻RV	ECUV1H020✻SV	ECUV1H020✻TV	ECUV1H020✻UV
3		ECUV1H030✻CV	ECUV1H030✻V	ECUV1H030✻PV	ECUV1H030✻RV	ECUV1H030✻SV	ECUV1H030✻TV	ECUV1H030✻UV
4		ECUV1H040✻CV	ECUV1H040✻V	ECUV1H040✻PV	ECUV1H040✻RV	ECUV1H040✻SV	ECUV1H040✻TV	ECUV1H040✻UV
5		ECUV1H050✻CV	ECUV1H050✻V	ECUV1H050✻PV	ECUV1H050✻RV	ECUV1H050✻SV	ECUV1H050✻TV	ECUV1H050✻UV
6	±0.5 pF (D)	ECUV1H060DCV	ECUV1H060DV	ECUV1H060DPV	ECUV1H060DRV	ECUV1H060DSV	ECUV1H060DTV	ECUV1H060DUV
7		ECUV1H070DCV	ECUV1H070DV	ECUV1H070DPV	ECUV1H070DRV	ECUV1H070DSV	ECUV1H070DTV	ECUV1H070DUV
8		ECUV1H080DCV	ECUV1H080DV	ECUV1H080DPV	ECUV1H080DRV	ECUV1H080DSV	ECUV1H080DTV	ECUV1H080DUV
9		ECUV1H090DCV	ECUV1H090DV	ECUV1H090DPV	ECUV1H090DRV	ECUV1H090DSV	ECUV1H090DTV	ECUV1H090DUV
10	±0.5 pF (D) or ±1 pf (F)	ECUV1H100✻CV	ECUV1H100✻V	ECUV1H100✻PV	ECUV1H100✻RV	ECUV1H100✻SV	ECUV1H100✻TV	ECUV1H100✻UV
12	±5%*** (J) or ±10% (K)	ECUV1H120✻CV	ECUV1H120✻V	ECUV1H120✻PV	ECUV1H120✻RV	ECUV1H120✻SV	ECUV1H120✻TV	ECUV1H120✻UV
15		ECUV1H150✻CV	ECUV1H150✻V	ECUV1H150✻PV	ECUV1H150✻RV	ECUV1H150✻SV	ECUV1H150✻TV	ECUV1H150✻UV
18		ECUV1H180✻CV	ECUV1H180✻V	ECUV1H180✻PV	ECUV1H180✻RV	ECUV1H180✻SV	ECUV1H180✻TV	ECUV1H180✻UV
22		ECUV1H220✻CV	ECUV1H220✻V	ECUV1H220✻PV	ECUV1H220✻RV	ECUV1H220✻SV	ECUV1H220✻TV	ECUV1H220✻UV
27		ECUV1H270✻CV	ECUV1H270✻V	ECUV1H270✻PV	ECUV1H270✻RV	ECUV1H270✻SV	ECUV1H270✻TV	ECUV1H270✻UV
33		ECUV1H330✻CV	ECUV1H330✻V	ECUV1H330✻PV	ECUV1H330✻RV	ECUV1H330✻SV	ECUV1H330✻TV	ECUV1H330✻UV
39		ECUV1H390✻CV	ECUV1H390✻V	ECUV1H390✻PV	ECUV1H390✻RV	ECUV1H390✻SV	ECUV1H390✻TV	ECUV1H390✻UV
47		ECUV1H470✻CV	ECUV1H470✻V	ECUV1H470✻PV	ECUV1H470✻RV	ECUV1H470✻SV	ECUV1H470✻TV	ECUV1H470✻UV
56		ECUV1H560✻CV	ECUV1H560✻V	ECUV1H560✻PV	ECUV1H560✻RV	ECUV1H560✻SV	ECUV1H560✻TV	ECUV1H560✻UV
68		ECUV1H680✻CV	ECUV1H680✻V	ECUV1H680✻PV	ECUV1H680✻RV	ECUV1H680✻SV	ECUV1H680✻TV	ECUV1H680✻UV
82		ECUV1H820✻CV	ECUV1H820✻V	ECUV1H820✻PV	ECUV1H820✻RV	ECUV1H820✻SV	ECUV1H820✻TV	ECUV1H820✻UV
100		ECUV1H101✻CV	ECUV1H101✻V	ECUV1H101✻PV	ECUV1H101✻RV	ECUV1H101✻SV	ECUV1H101✻TV	ECUV1H101✻UV
120		ECUV1H121✻CV	ECUV1H121✻V	ECUV1H121✻PV	ECUV1H121✻RV	ECUV1H121✻SV	ECUV1H121✻TV	ECUV1H121✻UV
150		ECUV1H151✻CV	ECUV1H151✻V	ECUV1H151✻PV	ECUV1H151✻RV	ECUV1H151✻SV	ECUV1H151✻TV	ECUV1H151✻UV
180		ECUV1H181✻CV	ECUV1H181✻V		ECUV1H181✻RV	ECUV1H181✻SV	ECUV1H181✻TV	ECUV1H181✻UV
220		ECUV1H221✻CV	ECUV1H221✻V				ECUV1H221✻TV	ECUV1H221✻UV
270		ECUV1H271✻CV	ECUV1H271✻V					ECUV1H271✻UV
330		ECUV1H331✻CV	ECUV1H331✻V					ECUV1H331✻UV
390		ECUV1H391✻CV	ECUV1H391✻V					ECUV1H391✻UV
470		ECUV1H471✻CV	ECUV1H471✻V					ECUV1H471✻UV
560		ECUV1H561✻CV	ECUV1H561✻V					ECUV1H561✻UV
680		ECUV1H681✻CV	ECUV1H681✻V					ECUV1H681✻UV
820		ECUV1H821✻CV	ECUV1H821✻V					ECUV1H821✻UV
1		ECUV1H102✻CV	ECUV1H102✻V					ECUV1H102✻UV
1200			ECUV1H122✻V					ECUV1H122✻UV

Packing style code*

Cap. Tol. Code**

* Packaging style code: "V" for taped version (taping pitch: 4mm) and "X" for bulk type

** ✻ : Capacitance tolerance codes

*** Capacitance values of "E24" series and capacitance tolerance of ±5% are available on special order.

■ Standard Products for "11" Type (EIA "0603" Type), Taped Version
Dim. T (mm) = 0.8

Cap. (pF)	Capacitance Tolerance	B/X7R		B/Y5P	Capacitance Tolerance	F/Y5V		
		50 VDC	25 VDC	16 VDC		50 VDC	25 VDC	16 VDC
		Part No.	Part No.	Part No.		Part No.	Part No.	Part No.
220		ECUV1H221✻BV						
270		ECUV1H271KBV						
330		ECUV1H331✻BV						
390		ECUV1H391KBV						
470		ECUV1H471✻BV						
560		ECUV1H561KBV						
680		ECUV1H681✻BV						
820		ECUV1H821KBV						
1000		ECUV1H102✻BV				ECUV1H102ZFV		
1200		ECUV1H122KBV						
1500		ECUV1H152✻BV				ECUV1H152ZFV		
1800		ECUV1H182KBV						
2200		ECUV1H222✻BV				ECUV1H222ZFV		
2700		ECUV1H272KBV						
3300		ECUV1H332✻BV				ECUV1H332ZFV		
3900		ECUV1H392KBV						
4700		ECUV1H472✻BV				ECUV1H472ZFV		
5600	±10% (K)	ECUV1H562KBV						
6800	or	ECUV1H682✻BV			+80/–20%	ECUV1H682ZFV		
8200	±20% (M)	ECUV1H822KBV			(Z)			
10,000		ECUV1H103✻BV		ECUV1C103✻BV		ECUV1H103ZFV		
12,000		ECUV1H123KBV		ECUV1C123KBV				
15,000		ECUV1H153✻BV		ECUV1C153✻BV		ECUV1H153ZFV		
18,000			ECUV1E183KBV	ECUV1C183KBV				
22,000			ECUV1E223✻BV	ECUV1C223✻BV		ECUV1H223ZFV		
27,000		Cap. Tol. code*	ECUV1E273KBV	ECUV1C273KBV				
33,000			ECUV1E333✻BV	ECUV1C333✻BV		ECUV1H333ZFV		
39,000				ECUV1C393KBV				
47,000				ECUV1C473✻BV		ECUV1H473ZFV		
56,000				ECUV1C563KBV				
68,000				ECUV1C683✻BV			ECUV1E683ZFV	
82,000				ECUV1C823KBV				
100,000				ECUV1C104✻BV			ECUV1E104ZFV	ECUV1C104ZFV
120,000								
150,000				Packing style code**				ECUV1C154ZFV
180,000								
220,000								ECUV1C224ZFV
270,000								
330,000								ECUV1C334ZFV
390,000								
470,000								ECUV1C472ZFV

* ✻ : Capacitance tolerance codes

** Packaging styles code: "V" for taped version (taping pitch: 4mm) and "X" for bulk type)

■ Standard Products for "11" Type (EIA "0603" Type), Taped Version
Dim. T (mm) = 0.8

Cap. (pF)	Capacitance Tolerance	B/X7R		B/Y5P	Capacitance Tolerance	F/Y5V		
		50 VDC	25 VDC	16 VDC		50 VDC	25 VDC	16 VDC
		Part No.	Part No.	Part No.		Part No.	Part No.	Part No.
220		ECUV1H221✻BV						
270		ECUV1H271KBV						
330		ECUV1H331✻BV						
390		ECUV1H391KBV						
470		ECUV1H471✻BV						
560		ECUV1H561KBV						
680		ECUV1H681✻BV						
820		ECUV1H821KBV						
1000		ECUV1H102✻BV				ECUV1H102ZFV		
1200		ECUV1H122KBV						
1500		ECUV1H152✻BV				ECUV1H152ZFV		
1800		ECUV1H182KBV						
2200		ECUV1H222✻BV				ECUV1H222ZFV		
2700		ECUV1H272KBV						
3300		ECUV1H332✻BV				ECUV1H332ZFV		
3900		ECUV1H392KBV						
4700		ECUV1H472✻BV				ECUV1H472ZFV		
5600	±10% (K)	ECUV1H562KBV						
6800	or	ECUV1H682✻BV			+80/–20%	ECUV1H682ZFV		
8200	±20% (M)	ECUV1H822KBV			(Z)			
10,000		ECUV1H103✻BV		ECUV1C103✻BV		ECUV1H103ZFV		
12,000		ECUV1H123KBV		ECUV1C123KBV				
15,000		ECUV1H153✻BV		ECUV1C153✻BV		ECUV1H153ZFV		
18,000			ECUV1E183KBV	ECUV1C183KBV				
22,000			ECUV1E223✻BV	ECUV1C223✻BV		ECUV1H223ZFV		
27,000		Cap. Tol. code*	ECUV1E273KBV	ECUV1C273KBV				
33,000			ECUV1E333✻BV	ECUV1C333✻BV		ECUV1H333ZFV		
39,000				ECUV1C393KBV				
47,000				ECUV1C473✻BV		ECUV1H473ZFV		
56,000				ECUV1C563KBV				
68,000				ECUV1C683✻BV			ECUV1E683ZFV	
82,000				ECUV1C823KBV				
100,000				ECUV1C104✻BV			ECUV1E104ZFV	ECUV1C104ZFV
120,000								
150,000				Packing style code**				ECUV1C154ZFV
180,000								
220,000								ECUV1C224ZFV
270,000								
330,000								ECUV1C334ZFV
390,000								
470,000								ECUV1C472ZFV

* ✻ : Capacitance tolerance codes

** Packaging styles code: "V" for taped version (taping pitch: 4mm) and "X" for bulk type)

■ Standard Products for "12" Type (EIA "0805" Type), Taped Version
[Rated Voltage 50 VDC]

Cap. (pF)	Cap. Tol.	Part Number															
		CΔ (NPO)	Dim. T (mm)	SL/GP	Dim. T (mm)	PΔ (N150)	Dim. T (mm)	RΔ (N220)	Dim. T (mm)	SΔ (N330)	Dim. T (mm)	TΔ (N470)	Dim. T (mm)	UΔ (N750)	Dim. T (mm)
0.5	±0.25 pF(C)	ECUV1H0R5CCN	0.6	ECUV1H0R5CN	0.6	ECUV1H0R5CPN	0.6	ECUV1H0R5CRN	0.6	ECUV1H0R5CSN	0.6	ECUV1H0R5CTN	0.6	ECUV1H0R5CUN	0.6
1	0.25 pF (C) or ±0.5 pF (D)	ECUV1H010✻CN	0.6	ECUV1H010✻N	0.6	ECUV1H010✻PN	0.6	ECUV1H010✻RN	0.6	ECUV1H010✻SN	0.6	ECUV1H010✻TN	0.6	ECUV1H010✻UN	0.6
1.5		ECUV1H1R5✻CN	0.6	ECUV1H1R5✻N	0.6	ECUV1H1R5✻PN	0.6	ECUV1H1R5✻RN	0.6	ECUV1H1R5✻SN	0.6	ECUV1H1R5✻TN	0.6	ECUV1H1R5✻UN	0.6
2		ECUV1H020✻CN	0.6	ECUV1H020✻N	0.6	ECUV1H020✻PN	0.6	ECUV1H020✻RN	0.6	ECUV1H020✻SN	0.6	ECUV1H020✻TN	0.6	ECUV1H020✻UN	0.6
3		ECUV1H030✻CN	0.6	ECUV1H030✻N	0.6	ECUV1H030✻PN	0.6	ECUV1H030✻RN	0.6	ECUV1H030✻SN	0.6	ECUV1H030✻TN	0.6	ECUV1H030✻UN	0.6
4		ECUV1H040✻CN	0.6	ECUV1H040✻N	0.6	ECUV1H040✻PN	0.6	ECUV1H040✻RN	0.6	ECUV1H040✻SN	0.6	ECUV1H040✻TN	0.6	ECUV1H040✻UN	0.6
5		ECUV1H050✻CN	0.6	ECUV1H050✻N	0.6	ECUV1H050✻PN	0.6	ECUV1H050✻RN	0.6	ECUV1H050✻SN	0.6	ECUV1H050✻TN	0.6	ECUV1H050✻UN	0.6
6	±0.5 pF (D)	ECUV1H060DCN	0.6	ECUV1H060DN	0.6	ECUV1H060DPN	0.6	ECUV1H060DRN	0.6	ECUV1H060DSN	0.6	ECUV1H060DTN	0.6	ECUV1H060DUN	0.6
7		ECUV1H070DCN	0.6	ECUV1H070DN	0.6	ECUV1H070DPN	0.6	ECUV1H070DRN	0.6	ECUV1H070DSN	0.6	ECUV1H070DTN	0.6	ECUV1H070DUN	0.6
8		ECUV1H080DCN	0.6	ECUV1H080DN	0.6	ECUV1H080DPN	0.6	ECUV1H080DRN	0.6	ECUV1H080DSN	0.6	ECUV1H080DTN	0.6	ECUV1H080DUN	0.6
9		ECUV1H090DCN	0.6	ECUV1H090DN	0.6	ECUV1H090DPN	0.6	ECUV1H090DRN	0.6	ECUV1H090DSN	0.6	ECUV1H090DTN	0.6	ECUV1H090DUN	0.6
10	±0.5 pF (D) or ±1 pf (F)	ECUV1H100✻CN	0.6	ECUV1H100✻N	0.6	ECUV1H100✻PN	0.6	ECUV1H100✻RN	0.6	ECUV1H100✻SN	0.6	ECUV1H100✻TN	0.6	ECUV1H100✻UN	0.6
12	±5%*** (J) or ±10% (K)	ECUV1H120✻CN	0.6	ECUV1H120✻N	0.6	ECUV1H120✻PN	0.6	ECUV1H120✻RN	0.6	ECUV1H120✻SN	0.6	ECUV1H120✻TN	0.6	ECUV1H120✻UN	0.6
15		ECUV1H150✻CN	0.6	ECUV1H150✻N	0.6	ECUV1H150✻PN	0.6	ECUV1H150✻RN	0.6	ECUV1H150✻SN	0.6	ECUV1H150✻TN	0.6	ECUV1H150✻UN	0.6
18		ECUV1H180✻CN	0.6	ECUV1H180✻N	0.6	ECUV1H180✻PN	0.6	ECUV1H180✻RN	0.6	ECUV1H180✻SN	0.6	ECUV1H180✻TN	0.6	ECUV1H180✻UN	0.6
22		ECUV1H220✻CN	0.6	ECUV1H220✻N	0.6	ECUV1H220✻PN	0.6	ECUV1H220✻RN	0.6	ECUV1H220✻SN	0.6	ECUV1H220✻TN	0.6	ECUV1H220✻UN	0.6
27		ECUV1H270✻CG	0.6	ECUV1H270✻G	0.6	ECUV1H270✻PN	0.6	ECUV1H270✻RN	0.6	ECUV1H270✻SN	0.6	ECUV1H270✻TN	0.6	ECUV1H270✻UN	0.6
33		ECUV1H330✻CG	0.6	ECUV1H330✻G	0.6	ECUV1H330✻PN	0.6	ECUV1H330✻RN	0.6	ECUV1H330✻SN	0.6	ECUV1H330✻TN	0.6	ECUV1H330✻UN	0.6
39		ECUV1H390✻CG	0.6	ECUV1H390✻G	0.6	ECUV1H390✻PN	0.6	ECUV1H390✻RN	0.6	ECUV1H390✻SN	0.6	ECUV1H390✻TN	0.6	ECUV1H390✻UN	0.6
47		ECUV1H470✻CG	0.6	ECUV1H470✻G	0.6	ECUV1H470✻PN	0.6	ECUV1H470✻RN	0.6	ECUV1H470✻SN	0.6	ECUV1H470✻TN	0.6	ECUV1H470✻UN	0.6
56		ECUV1H560✻CG	0.6	ECUV1H560✻G	0.6	ECUV1H560✻PN	0.6	ECUV1H560✻RN	0.6	ECUV1H560✻SN	0.6	ECUV1H560✻TN	0.6	ECUV1H560✻UN	0.6
68		ECUV1H680✻CG	0.6	ECUV1H680✻G	0.6	ECUV1H680✻PN	0.6	ECUV1H680✻RN	0.6	ECUV1H680✻SN	0.6	ECUV1H680✻TN	0.6	ECUV1H680✻UN	0.6
82		ECUV1H820✻CG	0.6	ECUV1H820✻G	0.6	ECUV1H820✻PN	0.6	ECUV1H820✻RN	0.6	ECUV1H820✻SN	0.6	ECUV1H820✻TN	0.6	ECUV1H820✻UN	0.6
100		ECUV1H101✻CG	0.6	ECUV1H101✻G	0.6	ECUV1H101✻PN	0.6	ECUV1H101✻RN	0.6	ECUV1H101✻SN	0.6	ECUV1H101✻TN	0.6	ECUV1H101✻UN	0.6
120		ECUV1H121✻CG	0.6	ECUV1H121✻G	0.6	ECUV1H121✻PN	0.6	ECUV1H121✻RN	0.6	ECUV1H121✻SN	0.6	ECUV1H121✻TN	0.6	ECUV1H121✻UN	0.6
150		ECUV1H151✻CG	0.6	ECUV1H151✻G	0.6	ECUV1H151✻PN	0.6	ECUV1H151✻RN	0.6	ECUV1H151✻SN	0.6	ECUV1H151✻TN	0.6	ECUV1H151✻UN	0.6
180		ECUV1H181✻CG	0.6	ECUV1H181✻G	0.6	ECUV1H181✻PN	0.6	ECUV1H181✻RN	0.6	ECUV1H181✻SN	0.6	ECUV1H181✻TN	0.6	ECUV1H181✻UN	0.6
220		ECUV1H221✻CG	0.6	ECUV1H221✻G	0.6	ECUV1H221✻PN	0.6	ECUV1H221✻RN	0.6	ECUV1H221✻SN	0.6	ECUV1H221✻TN	0.6	ECUV1H221✻UN	0.6
270		ECUV1H271✻CG	0.6	ECUV1H271✻G	0.6	ECUV1H271✻PN	0.6	ECUV1H271✻RN	0.85	ECUV1H271✻SN	0.85	ECUV1H271✻TN	0.6	ECUV1H271✻UN	0.6
330		ECUV1H331✻CG	0.6	ECUV1H331✻G	0.6	ECUV1H331✻PN	0.6	ECUV1H331✻RN	0.85	ECUV1H331✻SN	0.85	ECUV1H331✻TN	0.85	ECUV1H331✻UN	0.6
390		ECUV1H391✻CG	0.6	ECUV1H391✻G	0.6		0.6	ECUV1H391✻RN	0.85	ECUV1H391✻SN	0.85	ECUV1H391✻TN	0.85	ECUV1H391✻UX	0.6
470		ECUV1H471✻CX	0.6	ECUV1H471✻X	0.6		0.6			ECUV1H471✻SN	0.85	ECUV1H471✻TN	0.85	ECUV1H471✻UX	0.6
560		ECUV1H561✻CX	0.6	ECUV1H561✻X	0.6		0.6							ECUV1H561✻UX	0.6
680		ECUV1H681✻CX	0.6	ECUV1H681✻X	0.6		0.6							ECUV1H681✻UX	0.6
820		ECUV1H821✻CX	0.6	ECUV1H821✻X	0.6		0.6							ECUV1H821✻UX	0.6
1,000		ECUV1H102✻CX	0.6	ECUV1H102✻X	0.6		0.6							ECUV1H102✻UX	0.6
1,200		ECUV1H122✻CX	0.6	ECUV1H122✻X	0.6		0.6							ECUV1H122✻UX	0.6
1,500		ECUV1H152✻CX	0.6	ECUV1H152✻X	0.6		0.6							ECUV1H152✻UX	0.6
1,800		ECUV1H182✻CX	0.6	ECUV1H182✻X	0.6		0.6							ECUV1H182✻UX	0.6
2,200		ECUV1H222✻CX	0.6	ECUV1H222✻X	0.6		0.6							ECUV1H222✻UX	0.6
2,700		ECUV1H272✻CX	0.85	ECUV1H272✻X	0.85		0.6							ECUV1H272✻UX	0.6

Packing style code*

Cap. Tol. Code**

* Packaging style code: "V" for taped version (taping pitch: 4mm) and "X" for bulk type

** ✻ : Capacitance tolerance codes

*** Capacitance values of "E24" series and capacitance tolerance of ±5% are available on special order.

■ Standard Products for "12" Type (EIA "0805" Type), Taped Version

Cap. (pF)	Cap. Tol.	B/X7R				B/Y5P		Cap. Tol.	F/Y5V					
		50 VDC		25 VDC		16 VDC			50 VDC		25 VDC		16 VDC	
		Part No.	Dim. T (mm)	Part No.	Dim. T (mm)	Part No.	Dim. T (mm)		Part No.	Dim. T (mm)	Part No.	Dim. T (mm)	Part No.	Dim. T (mm)
220		ECUV1H221✻BN	0.6											
270		ECUV1H271✻BN	0.6											
330		ECUV1H331✻BN	0.6											
390		ECUV1H391KBN	0.6											
470		ECUV1H471✻BN	0.6											
560		ECUV1H561KBN	0.6											
680		ECUV1H681✻BN	0.6											
820		ECUV1H821KBN	0.6											
1,000		ECUV1H102✻BN	0.6						ECUV1H102ZFN	0.6				
1,,200		ECUV1H122KBN	0.6											
1,500		ECUV1H152✻BN	0.6						ECUV1H152ZFN	0.6				
1,800		ECUV1H182KBN	0.6											
2,200		ECUV1H222✻BN	0.6						ECUV1H222ZFN	0.6				
2,700		ECUV1H272KBN	0.6											
3,300		ECUV1H332✻BN	0.6						ECUV1H332ZFN	0.6				
3,900		ECUV1H392KBN	0.6											
4,700		ECUV1H472✻BG	0.6						ECUV1H472ZFN	0.6				
5,600	±10%	ECUV1H562KBG	0.6											
6,800	(K)	ECUV1H682✻BG	0.6					+80 –20%	ECUV1H682ZFN	0.6				
8,200	or	ECUV1H822KBG	0.6					(Z)						
10,000	±20%	ECUV1H103✻BG	0.6						ECUV1H103ZFG	0.6				
12,000	(M)	ECUV1H123KBX	0.6											
15,000		ECUV1H153✻BX	0.6						ECUV1H153ZFG	0.6				
18,000		ECUV1H183KBX	0.6	ECUV1E183KBX	0.6									
22,000		ECUV1H223✻BX	0.6	ECUV1E223✻BX	0.6				ECUV1H223ZFG	0.6				
27,000		ECUV1H273KBX	0.6	ECUV1E273KBX	0.6									
33,000		ECUV1H333✻BX	0.6	ECUV1E333✻BX	0.6				ECUV1H333ZFX	0.6				
39,000		ECUV1H393KBX	0.85	ECUV1E393KBX	0.6									
47,000				ECUV1E473✻BX	0.85	ECUV1C473✻BX	0.85		ECUV1H473ZFX	0.6				
56,000				ECUV1E563KBX	0.85	ECUV1C563KBX	0.85							
68,000		Cap. Tol. code*		ECUV1E683✻BX	0.85	ECUV1C683✻BX	0.85		ECUV1H683ZFX	0.6	ECUV1E683ZFX	0.6		
82,000				ECUV1E823KBX	0.85	ECUV1C823KBX	0.85							
100,000				ECUV1E104✻BX	0.85	ECUV1C104✻BX	0.85		ECUV1H104ZFC	0.85	ECUV1E104ZFX	0.6	ECUV1C104ZFX	0.6
120,000						ECUV1C124KBX	0.85							
150,000		Packing style code**				ECUV1C154✻BX	0.85				ECUV1E154ZFX	0.6	ECUV1C154ZFX	0.6
180,0000						ECUV1C184KBX	0.85							
220,000						ECUVC224✻BX	0.85				ECUV1E224ZFC	0.85	ECUV1C224ZFX	0.6
330,000													ECUV1C334ZFX	0.85
470,000													ECUV1C474ZFX	0.85
680,000													ECUV1C684ZFX	0.85
1,000,000													ECUV1C105ZFX	0.85

* ✻ : Capacitance tolerance codes

** Packaging styles code: "V" for taped version (taping pitch: 4mm) and "X" for bulk type)

■ Standard Products for "13" Type (EIA "1206" Type), Taped Version
[Rated Voltage 50 VDC]

Cap. (pF)	Cap. Tol.	Part Number															
		CΔ (NPO)	Dim. T (mm)	SL/GP	Dim. T (mm)	PΔ (N150)	Dim. T (mm)	RΔ (N220)	Dim. T (mm)	SΔ (N330)	Dim. T (mm)	TΔ (N470)	Dim. T (mm)	UΔ (N750)	Dim. T (mm)
0.5	±0.25 pF(C)	ECUV1H0R6CCM	0.6	ECUV1H0R6CM	0.6	ECUV1H0R6CPM	0.6	ECUV1H0R6CRM	0.6	ECUV1H0R6CSM	0.6	ECUV1H0R6CTM	0.6	ECUV1H0R6CUM	0.6
1	0.25 pF (C) or ±0.5 pF (D)	ECUV1H010✻CM	0.6	ECUV1H010✻M	0.6	ECUV1H010✻PM	0.6	ECUV1H010✻RM	0.6	ECUV1H010✻SM	0.6	ECUV1H010✻TM	0.6	ECUV1H010✻UM	0.6
1.5		ECUV1H1R5✻CM	0.6	ECUV1H1R5✻M	0.6	ECUV1H1R5✻PM	0.6	ECUV1H1R5✻RM	0.6	ECUV1H1R5✻SM	0.6	ECUV1H1R5✻TM	0.6	ECUV1H1R5✻UM	0.6
2		ECUV1H020✻CM	0.6	ECUV1H020✻M	0.6	ECUV1H020✻PM	0.6	ECUV1H020✻RM	0.6	ECUV1H020✻SM	0.6	ECUV1H020✻TM	0.6	ECUV1H020✻UM	0.6
3		ECUV1H030✻CM	0.6	ECUV1H030✻M	0.6	ECUV1H030✻PM	0.6	ECUV1H030✻RM	0.6	ECUV1H030✻SM	0.6	ECUV1H030✻TM	0.6	ECUV1H030✻UM	0.6
4		ECUV1H040✻CM	0.6	ECUV1H040✻M	0.6	ECUV1H040✻PM	0.6	ECUV1H040✻RM	0.6	ECUV1H040✻SM	0.6	ECUV1H040✻TM	0.6	ECUV1H040✻UM	0.6
5		ECUV1H050✻CM	0.6	ECUV1H050✻M	0.6	ECUV1H050✻PM	0.6	ECUV1H050✻RM	0.6	ECUV1H050✻SM	0.6	ECUV1H050✻TM	0.6	ECUV1H050✻UM	0.6
6	±0.5 pF (D)	ECUV1H060DCM	0.6	ECUV1H060DM	0.6	ECUV1H060DPM	0.6	ECUV1H060DRM	0.6	ECUV1H060DSM	0.6	ECUV1H060DTM	0.6	ECUV1H060DUM	0.6
7		ECUV1H070DCM	0.6	ECUV1H070DM	0.6	ECUV1H070DPM	0.6	ECUV1H070DRM	0.6	ECUV1H070DSM	0.6	ECUV1H070DTM	0.6	ECUV1H070DUM	0.6
8		ECUV1H080DCM	0.6	ECUV1H080DM	0.6	ECUV1H080DPM	0.6	ECUV1H080DRM	0.6	ECUV1H080DSM	0.6	ECUV1H080DTM	0.6	ECUV1H080DUM	0.6
9		ECUV1H090DCM	0.6	ECUV1H090DM	0.6	ECUV1H090DPM	0.6	ECUV1H090DRM	0.6	ECUV1H090DSM	0.6	ECUV1H090DTM	0.6	ECUV1H090DUM	0.6
10	±0.5 pF (D) or ±1 pf (F)	ECUV1H100✻CM	0.6	ECUV1H100✻M	0.6	ECUV1H100✻PM	0.6	ECUV1H100✻RM	0.6	ECUV1H100✻SM	0.6	ECUV1H100✻TM	0.6	ECUV1H100✻UM	0.6
12	±5%*** (J) or ±10% (K)	ECUV1H120✻CM	0.6	ECUV1H120✻M	0.6	ECUV1H120✻PM	0.6	ECUV1H120✻RM	0.6	ECUV1H120✻SM	0.6	ECUV1H120✻TM	0.6	ECUV1H120✻UM	0.6
15		ECUV1H150✻CM	0.6	ECUV1H150✻M	0.6	ECUV1H150✻PM	0.6	ECUV1H150✻RM	0.6	ECUV1H150✻SM	0.6	ECUV1H150✻TM	0.6	ECUV1H150✻UM	0.6
18		ECUV1H180✻CM	0.6	ECUV1H180✻M	0.6	ECUV1H180✻PM	0.6	ECUV1H180✻RM	0.6	ECUV1H180✻SM	0.6	ECUV1H180✻TM	0.6	ECUV1H180✻UM	0.6
22		ECUV1H220✻CM	0.6	ECUV1H220✻M	0.6	ECUV1H220✻PM	0.6	ECUV1H220✻RM	0.6	ECUV1H220✻SM	0.6	ECUV1H220✻TM	0.6	ECUV1H220✻UM	0.6
27		ECUV1H270✻CM	0.6	ECUV1H270✻M	0.6	ECUV1H270✻PM	0.6	ECUV1H270✻RM	0.6	ECUV1H270✻SM	0.6	ECUV1H270✻TM	0.6	ECUV1H270✻UM	0.6
33		ECUV1H330✻CM	0.6	ECUV1H330✻M	0.6	ECUV1H330✻PM	0.6	ECUV1H330✻RM	0.6	ECUV1H330✻SM	0.6	ECUV1H330✻TM	0.6	ECUV1H330✻UM	0.6
39		ECUV1H390✻CM	0.6	ECUV1H390✻M	0.6	ECUV1H390✻PM	0.6	ECUV1H390✻RM	0.6	ECUV1H390✻SM	0.6	ECUV1H390✻TM	0.6	ECUV1H390✻UM	0.6
47		ECUV1H470✻CM	0.6	ECUV1H470✻M	0.6	ECUV1H470✻PM	0.6	ECUV1H470✻RM	0.6	ECUV1H470✻SM	0.6	ECUV1H470✻TM	0.6	ECUV1H470✻UM	0.6
56		ECUV1H560✻CM	0.6	ECUV1H560✻M	0.6	ECUV1H560✻PM	0.6	ECUV1H560✻RM	0.6	ECUV1H560✻SM	0.6	ECUV1H560✻TM	0.6	ECUV1H560✻UM	0.6
68		ECUV1H680✻CM	0.6	ECUV1H680✻M	0.6	ECUV1H680✻PM	0.6	ECUV1H680✻RM	0.6	ECUV1H680✻SM	0.6	ECUV1H680✻TM	0.6	ECUV1H680✻UM	0.6
82		ECUV1H820✻CM	0.6	ECUV1H820✻M	0.6	ECUV1H820✻PM	0.6	ECUV1H820✻RM	0.6	ECUV1H820✻SM	0.6	ECUV1H820✻TM	0.6	ECUV1H820✻UM	0.6
100		ECUV1H101✻CH	0.6	ECUV1H101✻H	0.6	ECUV1H101✻PM	0.6	ECUV1H101✻RM	0.6	ECUV1H101✻SM	0.6	ECUV1H101✻TM	0.6	ECUV1H101✻UM	0.6
120		ECUV1H121✻CH	0.6	ECUV1H121✻H	0.6	ECUV1H121✻PM	0.6	ECUV1H121✻RM	0.6	ECUV1H121✻SM	0.6	ECUV1H121✻TM	0.6	ECUV1H121✻UM	0.6
150		ECUV1H151✻CH	0.6	ECUV1H151✻H	0.6	ECUV1H151✻PM	0.6	ECUV1H151✻RM	0.6	ECUV1H151✻SM	0.6	ECUV1H151✻TM	0.6	ECUV1H151✻UM	0.6
180		ECUV1H181✻CH	0.6	ECUV1H181✻H	0.6	ECUV1H181✻PM	0.6	ECUV1H181✻RM	0.6	ECUV1H181✻SM	0.6	ECUV1H181✻TM	0.6	ECUV1H181✻UM	0.6
220		ECUV1H221✻CH	0.6	ECUV1H221✻H	0.6	ECUV1H221✻PM	0.6	ECUV1H221✻RM	0.6	ECUV1H221✻SM	0.6	ECUV1H221✻TM	0.6	ECUV1H221✻UM	0.6
270		ECUV1H271✻CH	0.6	ECUV1H271✻H	0.6	ECUV1H271✻PM	0.6	ECUV1H271✻RM	0.6	ECUV1H271✻SM	0.6	ECUV1H271✻TM	0.6	ECUV1H271✻UM	0.6
330		ECUV1H331✻CH	0.6	ECUV1H331✻H	0.6	ECUV1H331✻PM	0.6	ECUV1H331✻RM	0.6	ECUV1H331✻SM	0.6	ECUV1H331✻TM	0.6	ECUV1H331✻UM	0.6
390		ECUV1H391✻CH	0.6	ECUV1H391✻H	0.6	ECUV1H391✻PM	0.6	ECUV1H391✻RM	0.6	ECUV1H391✻SM	0.6	ECUV1H391✻TM	0.6	ECUV1H391✻UM	0.6
470		ECUV1H471✻CH	0.6	ECUV1H471✻H	0.6	ECUV1H471✻PM	0.6	ECUV1H471✻RM	0.6	ECUV1H471✻SM	0.6	ECUV1H471✻TM	0.6	ECUV1H471✻UM	0.6
560		ECUV1H561✻CH	0.6	ECUV1H561✻H	0.6	ECUV1H561✻PM	0.6	ECUV1H561✻RM	0.6	ECUV1H561✻SM	0.6	ECUV1H561✻TM	0.6	ECUV1H561✻UM	0.6
680		ECUV1H681✻CH	0.6	ECUV1H681✻H	0.6	ECUV1H681✻PM	0.85	ECUV1H681✻RM	0.85	ECUV1H681✻SM	0.6	ECUV1H681✻TM	0.6	ECUV1H681✻UM	0.6
820		ECUV1H821✻CH	0.6	ECUV1H821✻H	0.6	ECUV1H821✻PM	0.85	ECUV1H821✻RM	0.85	ECUV1H821✻SM	0.85	ECUV1H821✻TM	0.6	ECUV1H821✻UM	0.6
1,000		ECUV1H102✻CH	0.6	ECUV1H102✻H	0.6	ECUV1H102✻PM	0.85	ECUV1H102✻RM	0.85	ECUV1H102✻SM	0.85	ECUV1H102✻TM	0.85	ECUV1H102✻UM	0.6
1,200		ECUV1H122✻CW	0.6	ECUV1H122✻W	0.6	ECUV1H122✻PM	0.85	ECUV1H122✻RM	0.85	ECUV1H122✻SM	0.85	ECUV1H122✻TM	0.85	ECUV1H122✻UM	0.6
1,500		ECUV1H152✻CW	0.6	ECUV1H152✻W	0.6	ECUV1H152✻PM	1.15	ECUV1H152✻RM	1.15	ECUV1H152✻SM	0.85	ECUV1H152✻TM	0.85	ECUV1H152✻UW	0.6
1,800		ECUV1H182✻CW	0.6	ECUV1H182✻W	0.6					ECUV1H182✻SM	1.15	ECUV1H182✻TM	1.15	ECUV1H182✻UW	0.6
2,200		ECUV1H222✻CW	0.6	ECUV1H222✻W	0.6							ECUV1H222✻TM	1.15	ECUV1H222✻UW	0.6
2,700		ECUV1H272✻CW	0.6	ECUV1H272✻W	0.6									ECUV1H272✻UW	0.6
3,300		ECUV1H332✻CW	0.6	ECUV1H332✻W	0.6									ECUV1H332✻UW	0.6
3,900		ECUV1H392✻CW	0.6	ECUV1H392✻W	0.6									ECUV1H392✻UW	0.6
4,700		ECUV1H472✻CW	0.6	ECUV1H472✻W	0.6									ECUV1H472✻UW	0.6
5,600		ECUV1H562✻CW	0.85	ECUV1H562✻W	0.6									ECUV1H562✻UW	0.6
6,800		ECUV1H682✻CW	0.85												
8,200		ECUY1H822✻CW	1.15												
10,000		ECUY1H103✻CW	1.15												

Packing style code*

Cap. Tol. Code**

■ Standard Products for "13" Type (EIA "1206" Type), Taped Version

Cap. (pF)	Cap. Tol.	B/X7R				B/Y5P		Cap. Tol.	F/Y5V					
		50 VDC		25 VDC		16 VDC			50 VDC		25 VDC		16 VDC	
		Part No.	Dim. T (mm)	Part No.	Dim. T (mm)	Part No.	Dim. T (mm)		Part No.	Dim. T (mm)	Part No.	Dim. T (mm)	Part No.	Dim. T (mm)
220		ECUV1H221✻BM	0.6											
270		ECUV1H271✻BM	0.6											
330		ECUV1H331✻BM	0.6											
390		ECUV1H391KBM	0.6											
470		ECUV1H471✻BM	0.6											
560		ECUV1H561KBM	0.6											
680		ECUV1H681✻BM	0.6											
820		ECUV1H821KBM	0.6											
1,000		ECUV1H102✻BM	0.6						ECUV1H102ZFM	0.6				
1,200		ECUV1H122KBM	0.6											
1,500		ECUV1H152✻BM	0.6						ECUV1H152ZFM	0.6				
1,800		ECUV1H182KBM	0.6											
2,200		ECUV1H222✻BM	0.6						ECUV1H222ZFM	0.6				
2,700		ECUV1H272KBM	0.6											
3,300		ECUV1H332✻BM	0.6						ECUV1H332ZFM	0.6				
3,900		ECUV1H392KBM	0.6											
4,700		ECUV1H472✻BM	0.6						ECUV1H472ZFM	0.6				
5,600	±10%	ECUV1H562KBM	0.6											
6,800	(K)	ECUV1H682✻BM	0.6					+80 –20% (Z)	ECUV1H682ZFM	0.6				
8,200	or	ECUV1H822KBM	0.6											
10,000	±20%	ECUV1H103✻BM	0.6						ECUV1H103ZFM	0.6				
12,000	(M)	ECUV1H123KBM	0.6											
15,000		ECUV1H153✻BM	0.6						ECUV1H153ZFM	0.6				
18,000		ECUV1H183KBM	0.6											
22,000		ECUV1H223✻BM	0.6						ECUV1H223ZFM	0.6				
27,000		ECUV1H273KBW	0.6											
33,000		ECUV1H333✻BW	0.6	ECUV1E333✻BW	0.6				ECUV1H333ZFM	0.6				
39,000		ECUV1H393KBW	0.85	ECUV1E393KBW	0.6									
47,000		ECUV1H473✻BW		ECUV1E473✻BW	0.6		0.85		ECUV1H473ZFM	0.6				
56,000		ECUV1H563KBW		ECUV1E563KBW	0.6		0.85							
68,000		ECUV1H683✻BW		ECUV1E683✻BW	0.6		0.85		ECUV1H683ZFW	0.6				
82,000		ECUV1H823KBW		ECUV1E823KBW	0.6		0.85							
100,000		ECUV1H104✻BW		ECUV1E104✻BW	0.85	ECUV1C104✻BW	0.85		ECUV1H104ZFW	0.6	ECUV1E104ZFW	0.6		
120,000				ECUV1E124KBW	0.85	ECUV1C124KBW	0.85							
150,000				ECUV1E154✻BW	0.85	ECUV1C154✻BW	0.85		ECUV1H154ZFW	0.6	ECUV1E154ZFW	0.6		
180,000		Cap. Tol. code*		ECUV1E184KBW	0.85	ECUV1C184KBW	0.85							
220,000				ECUV1E224✻BW	0.85	ECUVC224✻BW	0.85		ECUV1H224ZFW	0.6	ECUV1E224ZFW	0.6		
270,000						ECUV1C274KBW								
330,000		Packing style code**				ECUV1C334✻BW					ECUV1E334ZFW	0.6		
390,000						ECUV1C394KBW								
470,000						ECUVC474✻BW					ECUV1E474ZFW	0.6		
560,000						ECUV1C564KBW								
680,000						ECUV1C684✻BW							ECUV1C684ZFW	0.85
820,000						ECUY1C824KBW								
1,000,000						ECUYC105✻BW							ECUV1C105ZFW	0.85
1,500,000													ECUV1C155ZFW	0.85
2,200,000													ECUV1C225ZFW	0.85

■ Packaging Specifications

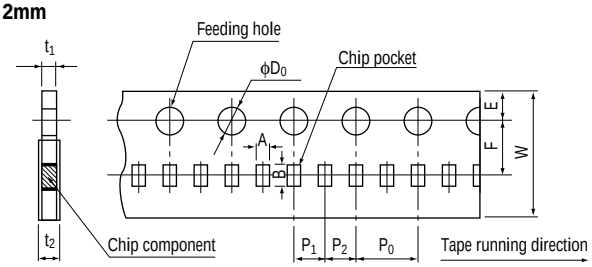
Standard Packing Quantity

Size Code	Thickness	Paper Taping	Embossed Taping	Bulk	Bulk Case
10 (0402)	0.5mm	Pitch 2mm: 10,000 (50,000) pcs./reel	—	1,000 pcs./bag	50,000 pcs./case
11 (0603)	0.8mm	Pitch 2mm: 8,000 (20,000) pcs./reel	—	1,000 pcs./bag	15,000 pcs./case
		Pitch 4mm: 4,000 (10,000) pcs./reel	—	1,000 pcs./bag	
12 (0805)	0.6mm	Pitch 2mm: 10,000 (40,000) pcs./reel	—	1,000 pcs./bag	10,000 pcs./case
		Pitch 4mm: 5,000 (20,000) pcs./reel	—	1,000 pcs./bag	
	0.85mm	Pitch 4mm: 4,000 (10,000) pcs./reel	—	1,000 pcs./bag	—
	1.25mm	—	—	1,000 pcs./bag	—
13 (1206)	0.6mm	Pitch 4mm: 5,000 (20,000) pcs./reel	—	1,000 pcs./bag	—
	0.85mm	Pitch 4mm: 4,000 (10,000) pcs./reel	—	1,000 pcs./bag	—
	1.15mm	—	Pitch 4mm: 2,000 (10,000) pcs./reel	1,000 pcs./bag	—

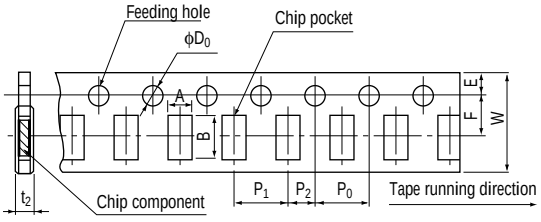
( ) for large size reel applied

Paper Taping

P_1: 2mm



P_1: 4mm



Type	Dimensions					
	A	B	W	F	E	P_1
10 (0402)	0.65 ±0.05	1.15 ±0.05	8.0 ±0.2	3.50 ±0.05	1.75 ±0.10	2.00 ±0.05
11 (1603)	1.10 ±0.10	1.90 ±0.10				
12 (0805)	1.65 ±0.20	2.4 ±0.2				

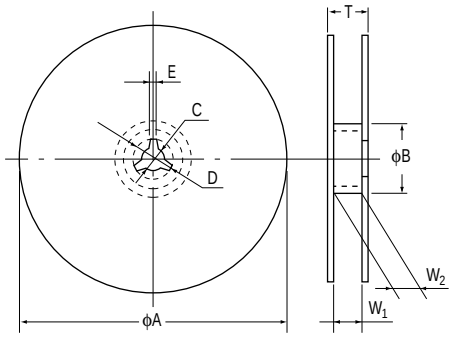
Type	P_2	P_0	φD_0	t_1	t_2
10 (0402)	2.00 ±0.05	4.0 ±0.1	1.5 ±0.1/0	0.7 max.	1.0 max.
11 (1603)				1.1 max.	1.4 max.
12 (0805)					

Type	Dimensions					
	A	B	W	F	E	P_1
11 (1206)	1.10 ±0.10	1.90 ±0.10	8.0 ±0.2	3.50 ±0.05	1.75 ±0.10	4.0 ±0.1
12 (1206)	1.65 ±0.20	2.4 ±0.2				
13 (1206)	2.0 ±0.2	3.6 ±0.2				

Type	P_2	P_0	φD_0	t_1	t_2
11 (1206)	2.00 ±0.05	4.0 ±0.1	1.5 ±0.1/0	1.1 max.	1.4 max.
12 (1206)					
13 (1206)					

■ Packaging Specifications *(cont'd)*

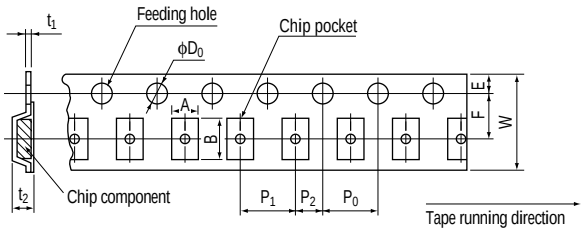
Reel for Taping



Dimensions						
A	B	C	D	E	W_1	W_0
$\varphi 180^{0/-1}$ ($330^{\pm 5}$)	$\varphi 60^{\pm 0.5}$ (50 min.)	$13.0^{\pm 0.5}$	$21.0^{\pm 0.8}$ (20 min.)	$2.0^{\pm 0.5}$	$9.0^{\pm 0.3}$ ($9.5^{\pm 1.0}$)	$1.3^{\pm 0.2}$ ($2.0^{\pm 0.5}$)

( ): Large size taping reel

Embossed Taping

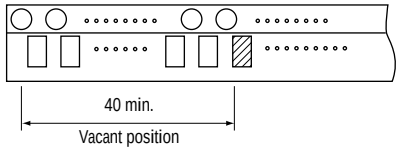


Type	Dimensions A	B	W	F	E	P 1
13 (1206)	1.95 ±0.20	3.6 ±0.2	8.0 ±0.2	3.50 ±0.05	1.75 ±0.10	4.0 ±0.1

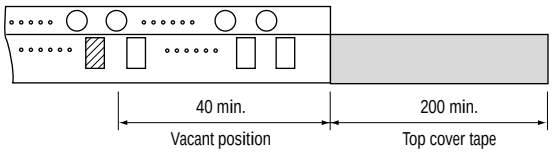
Type	P 2	P 0	φD0	t 1	t 2
13 (1206)	2.00 ±0.05	4.0 ±0.1	1.5 ±0.1/0	0.6 max.	1.5 max.

Leader Park and Taped End

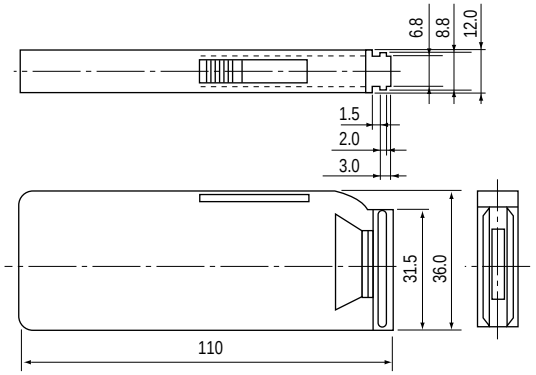
Tape end



Leader part



Bulk Case

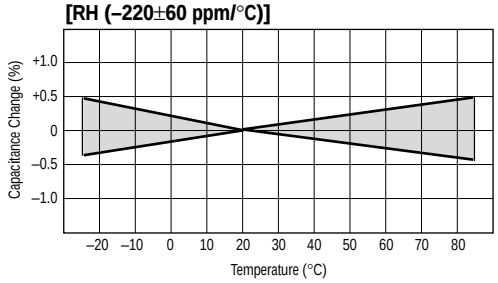


Unit: mm

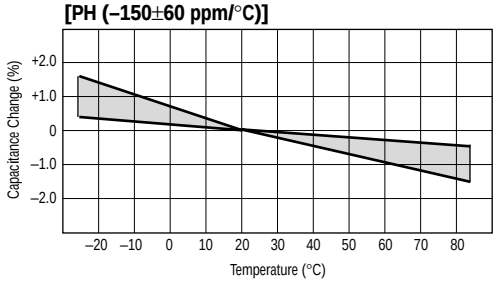
■ Typical Temperature Characteristics

Class 1 (T.C. Type)

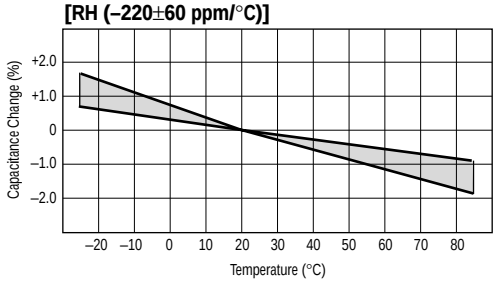
[RH (–220±60 ppm/°C)]



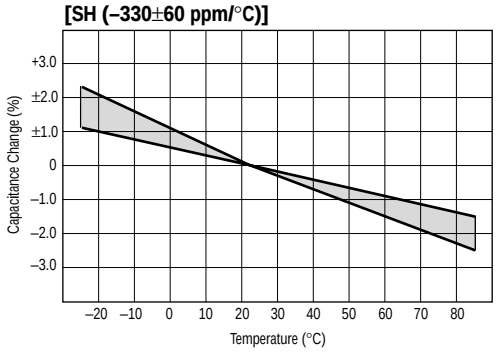
[PH (–150±60 ppm/°C)]



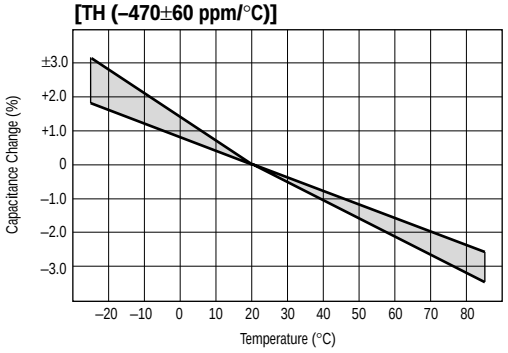
[RH (–220±60 ppm/°C)]



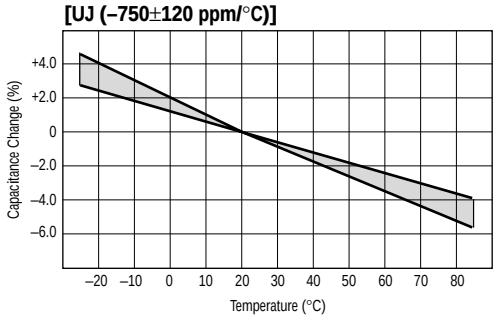
[SH (–330±60 ppm/°C)]



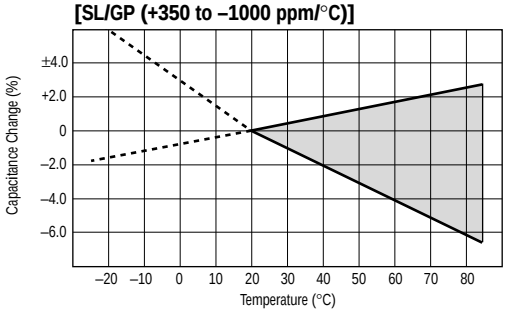
[TH (–470±60 ppm/°C)]



[UJ (–750±120 ppm/°C)]

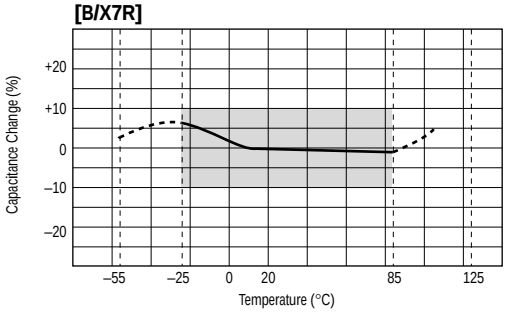


[SL/GP (+350 to –1000 ppm/°C)]

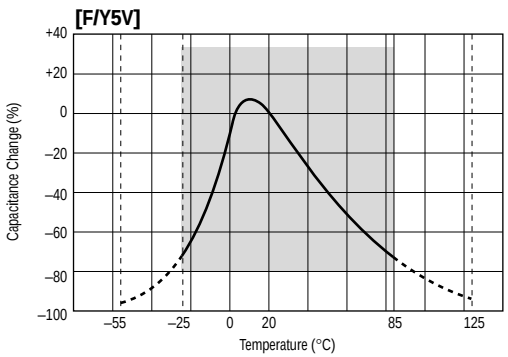


Class 2 (Hi-K Type)

[B/X7R]



[F/Y5V]



Safety Precautions

Series: ECU

The Multilayer Ceramic Chip Capacitors (hereafter referred to as "The Capacitors" may fail in a short circuit mode in an open-circuit mode, when subjected to severe conditions of electrical, environmental, and/or mechanical stresses beyond the specified "Ratings" and specified "Conditions" in the catalog and the specifications, resulting in burnout, flaming, or glowing in the worst case.

■ Packaging Specifications

1.1 Operating Temperature Range

The specified "Operating Temperature Range" in this catalog is absolute maximum and minimum temperature rating. So, in any case, each of the capacitors should be operated within the specified operating temperature range.

1.2 Designs of Voltage Applications

The capacitors should not be operated exceeding the specified rated voltage in this catalog. If voltage ratings are exceeded, the capacitors could result in failure or damage. In case of application of DC and AC voltage to the capacitors, the designed peak voltage to the capacitors, the designed peak voltage should be within the specified rated voltage.

In case of AC pulse voltage, the peak voltage (peak to peak) should be within the specified rated voltage. If high frequency voltage or fast-rising pulse voltage is applied continuously even within the rated voltage, contact our engineering section before use.

1.3 Charging and Discharging Current

The capacitors should not be operated beyond the specified "maximum charging/discharging current ratings" in the specifications. Applications to a low impedance circuit such as a "secondary power circuit" are not recommended for safety.

1.4 Temperature Rise by Dielectric Loss of the Capacitor

The "Operating Temperature Range" mentioned above shall include a maximum surface temperature rise of 20°C, which is caused by the dielectric loss of the capacitor and applied electrical stresses (such as voltage, frequency, and wave form, etc.).

It is recommended to measure and check "surface temperature of the capacitor" in your equipment at your estimated/designed maximum ambient temperature.

1.5 Restriction on Environmental Conditions

The capacitors should not be operated and/or stored under the following environmental conditions:

- Direct exposure to water or salt water
- Direct exposure to sunlight
- Under conditions of dew formation
- Under conditions of corrosive atmospheres such as hydrogen sulfide, sulfurous acid, chlorine, or ammonia.
- Under severe conditions of vibrations or shock beyond the specified conditions in the specifications.

1.6 Secular Changes in Capacitance

(1) Peculiar characteristics of "secular changes in capacitance" are observed in the capacitors (class 2 high dielectric constant. Temperature characteristics "X7R" and "Y5V"). The "secular changes" shall be considered in your circuit design.

(2) The capacitance changes, due to the individual characteristics or ceramic dielectric materials applied, can be recovered to each initial value at shipping by a heat treatment (140° to 150°C for one hour).

(The recovered capacitance of Class 2 capacitor shall be measured at the standard test condition after recovery times of 48 hours.)

■ Design of Printed Circuit Board

2.1 Selection of Printed Circuit Boards

When the capacitors are mounted and soldered on an "aluminum substrate," the substrate has influences on capacitor's reliability against "temperature cycles" and "heat shock" because of difference of thermal expansion coefficient between them. It should be carefully confirmed that the actual board supplied does not deteriorate the characteristics of the capacitors.

2.2 Design of Land Pattern

- Recommended dimensions of lands: As shown below in Figure 1 and Table 1.

  Note: Too large land requires excess amount of solder. The dimensions should be symmetrical.

Figure 1
Recommended Land Dimensions

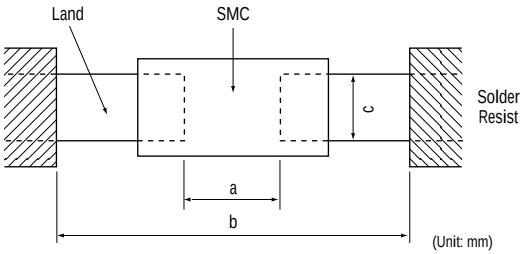


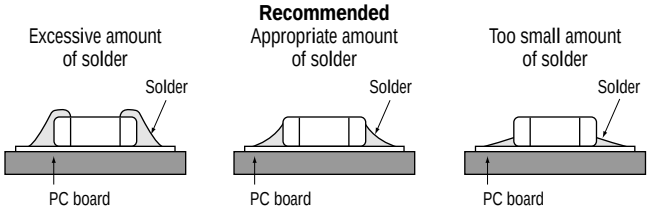
Table 1
Recommended Land Dimensions in mm

Size Code (EIA)	Component DImensions			Land Dimensions for Flow Soldering			Land Dimensions for Reflow Soldering		
	L	W	T	a	b	c	a	b	c
13 (1206)	3.2	1.6	0.5–1.25	2.0–2.4	4.4–4.8	1.0–1.3	1.8–2.4	3.8–4.8	1.2–1.6
12 (0805)	2.0	1.25	0.5–1.45	1.0–1.4	3.0–3.2	0.8–1.0	0.8–1.2	2.4–3.2	1.0–1.2
11 (0603)	1.6	0.8	0.8	0.8–1.0	2.0–2.6	0.6–0.8	0.8–1.0	2.0–2.6	0.8–1.0
10 (0402)	1.0	0.5	0.5	—	—	—	0.5–0.6	1.5–1.7	0.5–0.6

2.2 Design of Land Pattern *(cont'd)*

- Recommended amount of solder (shown in Figure 2). Excessive amount of solder gives large mechanical stresses to the capacitors/components.

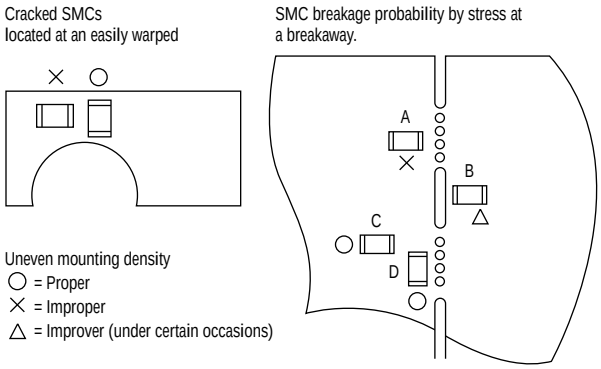
Figure 2.
Recommended Amount of Solder



2.3 Component Layout

When placing/mounting the capacitors/components near an area which is apt to bend or a grid groove on the PC board, it is advisable to have both electrodes subjected to uniform stresses, or to position the components' electrodes at right angles to the gride groove or bending line.

Figure 3
Component Layout



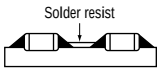
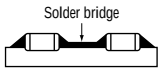
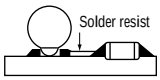
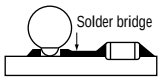
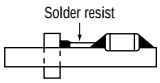
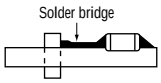
Probability at which the chip capacitor is broken by the stress on PC board break:
A > C > B ≒ D

2.4 Mounting Density and Spaces

Placement in too narrow spaces between components may cause "solder bridges" during soldering. The minimum space between components should be 0.5mm in view of the positioning tolerances of the mounting machines and the dimensional tolerances of components and PC boards.

2.5 Applications of Solder Resist

Applications of solder resist are effective to prevent solder bridges and to control amounts of solder on PC boards and shown in the following table.

	Recommended Application Examples	Examples of Solder Bridges
Narrow spacing between chip components		
Radial components are directly connected to chip components		
Common lands (chassis, etc.) are close to chip components		

■ Precautions for Assembly

3.1 Adhesives for Mounting

Selection of adhesives

- The viscosity of an adhesive for mountings shall be such that the adhesive does not flow off on the land during its curing.
- If the adhesive is too low in its viscosity, mounted components may be out of alignment after or during soldering.
- The adhesives shall not be corrosive or chemically active to the mounted components and the PC boards.
- The amount of adhesive shall be such that the adhesive does not flow off or be out of alignment.

Curing Conditions

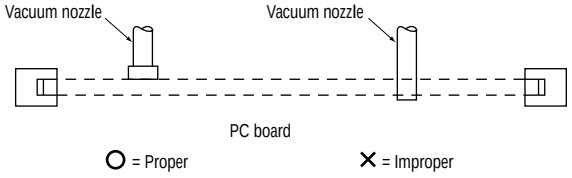
- Adhesives for mountings can be cured by ultraviolet or infrared radiation. In order to prevent the terminal electrodes of the capacitors from oxidizing, the curing shall be done at conditions of 160°C max., for two (2) minutes max.

3.2 Chip Mounting Considerations

In mounting the capacitors/components on a printed circuit board, any bending and expanding force against them should be kept to a minimum to prevent them from becoming damaged or cracked.

- Maximum stroke of the vacuum nozzle should be adjusted so the pushing force to the printed circuit board should be limited to a static board of 1 to 3N (100 to 300 gf). (See Figure 4.)

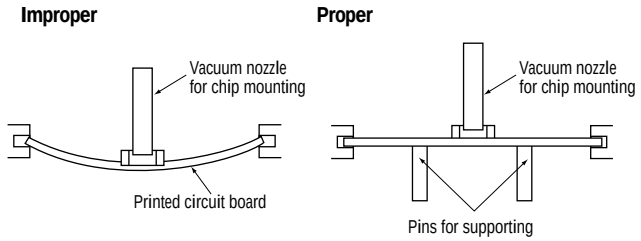
Figure 4



3.2 Chip Mounting Considerations *(cont'd)*

- The printed circuit board should be supported by means of adequate supporting pins as shown in Figure 5.

Figure 5



3.3 Soldering Flux and Solder

Soldering Flux

- The content of halogen in the soldering flux should be 0.2 wt% or less.
- Rosin-based and non-activated soldering flux is recommended.

Water soluble type soldering flux

- In case of water soluble type soldering flux being applied, the flux residue on the surface of PC boards may have influences on the reliability of the components and cause deterioration and failures of them.

Solder

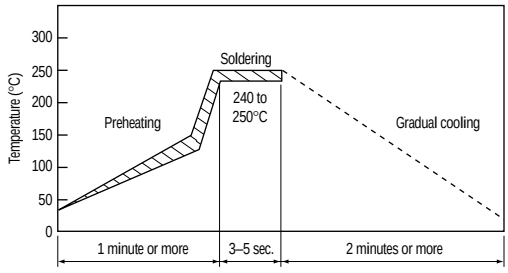
- And eutetic solder (Sn63: Pb37) is recommended.

3.4 Soldering

Flow soldering

In the flow soldering process, abnormal and large thermal and mechanical stresses, caused by "temperature gradient" between the mounted capacitors and melted solder in a soldering bath, may be applied directly to the capacitors, resulting in failures and damages of the capacitors. So it is essential that the soldering process be controlled to the following recommended conditions and precautions. (See Figure 6.)

Figure 6
Recommended Soldering Temperature–Time Profile (Flow Soldering)

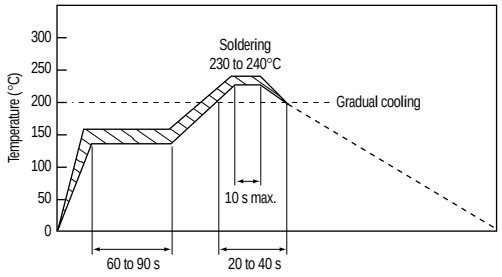


- Application of flux: The soldering flux (3.3) should be applied to the mounted capacitors thinly and uniformly by forming method.
- Preheating. The mounted capacitors/components should be preheated sufficiently so that the "temperature gradient" between the capacitors/components and melted solder is 150°C or below.
- Immersion of soldering bath. The capacitors should be cooled gradually to room ambient temperature with the cooling temperature rates of 8°C/s max. from 250°C to 170°C, and 4°C/s max. from 170°C to 130°C.
- Flux cleaning. When the capacitors are immersed into cleaning solvent, it should be confirmed that the surface temperatures of devices do not exceed 100°C (see section 3.5).

Reflow soldering

In the reflow soldering process, the mounted capacitors/components are generally heated and soldered by a thermal conduction system such as an "infrared radiation and hot blast soldering system" or a "vapor phase soldering system (VPS)." Large temperature gradients such as a rapid heating and cooling in the process may cause electrical failures and mechanical damages of the device. It is essential that the soldering process be controlled by the following recommended conditions and precautions. (See Figure 7.)

Figure 7
Recommended Soldering Temperature–Time Profile (Reflow Soldering)



- Preheating 1: Capacitors/components should be preheated sufficiently, for 60 to 90 seconds so that the surface temperature of them is 140° to 160°C.
- Preheating 2: After "Preheating 1," the mounted capacitors/components should be heated to the elevated temperatures of 150° to 200°C for 2 to 5 seconds.
- Soldering. The mounted capacitors/components should be heated under the specified heating conditions (200 to 240 to 200°C for a total of 20 to 40 seconds; see Figure 7) and should be soldered at the maximum temperature of 240° for 10 seconds or less.
- Cooling. After the soldering, the mounted capacitors/components should be gradually cooled to room ambient temperature for preventing mechanical damages such as cracking of the devices.
- Flux cleaning. When the mounted capacitors/components are immersed into cleaning solvent, it shall be confirmed that the surface temperature of them do not exceed 100°C. (See 3.5, Post Soldering Cleaning.)

Note: If the mounted capacitors/components are partially heated in the soldering process, the devices may be separated from the printed circuit board by the surface tension of partially melted solder, and stand up like a "tombstone."

Hand Soldering

In hand soldering of the capacitors, large temperature gradient between preheated capacitors and the tip of soldering iron may cause electrical failures and mechanical damages such as cracking or breaking of the devices. The soldering should be carefully controlled and carried out so that the temperature gradient is kept minimum with following recommended conditions for hand soldering.

- Solder. φ1mm thread eutetic solder (Sn63: Pb37) with soldering flux* in the core.
  * Rosin-based, and non-activated flux is recommended
- Preheating. The capacitors should be preheated so that "temperature gradient" between the devices and the tip of soldering iron is 150°C or below.
- Soldering iron. Rated power of 20W max. with 3m soldering tip in diameter.
- Temperature of soldering iron tip: 300°C max. (The required amount of solder should be melted in advance on the soldering tip.)
- Cooling. After soldering, the capacitors should be cooled gradually at room ambient temperature.

3.5 Post Soldering Cleaning

- Residues of corrosive soldering fluxes on the PC board after cleaning may greatly have influences on the electrical characteristics and the reliability (such as humidity resistance) of the capacitors which have been mounted on the board, it should be confirmed that the characteristics and the reliability of the devices are not affected by the applied cleaning conditions.
- Solubility of alternative cleaning solvent (such as alcohol) is inferior to that of freon cleaning solvent in the flux cleaning. So, in the case of alternative cleaning solvents applied, fresh cleaning solvent should always be used, followed by sufficient rinsing and drying.
- When an ultrasonic cleaning is applied to the mounted capacitors on PC boards, following conditions are recommended for preventing failures or damages of the devices due to the large vibration energy and the resonance caused by the ultrasonic waves.

Frequency	: 20 kHz max.
Radiated power	: 20 W/liter max.
Period	: 5 minutes max.

3.6 Process Inspection

When the mounted printed circuits are inspected with measuring terminal pins, abnormal and excess mechanical stresses should not be applied to the PC board and mounted components, in order to prevent failure of or damage to the devices.

- The mounted PC boards should be supported by some adequate supporting pins to prevent bending.
- Confirm that measuring pins have the right tip in place, that they are equal in height, and are set in the right positions.

3.7 Protective Coating

When the surface of a printed board on which the capacitors have been mounted is coated with resin to protect against moisture and dust, it should be confirmed that the protective coat does not have influences on reliability of the capacitors in the actual equipment.

- Coating materials, such as being corrosive and chemically active, should not be applied to the capacitors and other components.
- Coating materials with large expansivity should not be applied to the capacitors for preventing failures or damages (such as cracking) of the devices in the curing process.

3.8 Dividing/Breaking of PC Boards

- Abnormal and excessive mechanical stresses, such as bending or expanding force, on the components on the printed circuit board, should be kept minimum in the dividing/breaking.
- Dividing/breaking of the PC boards should be done carefully at moderate speed by using a jig or apparatus to prevent the capacitors on the boards from mechanical damages.

3.9 Long-Term Storage

The capacitors shall not be stored under severe conditions of high temperatures and high humidity. Store them indoors with 40°C max. and 75% RH max. Use them within six (6) months and check the solderability before use (see section 1.5).